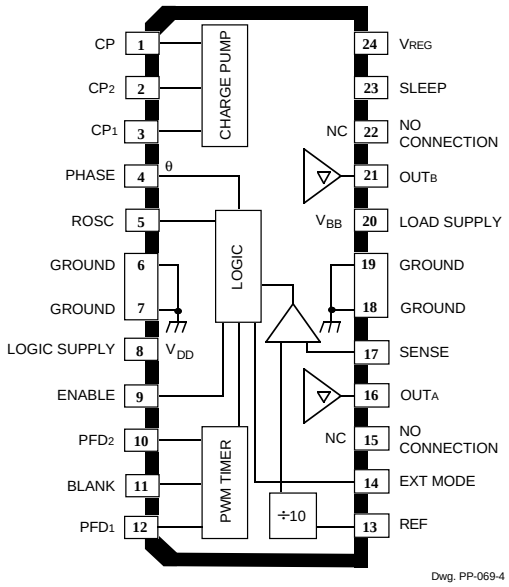
3959

Data Sheet
29319.37

PRELIMINARY INFORMATION
(subject to change without notice)
April 23, 2002

DMOS FULL-BRIDGE PWM MOTOR DRIVER

A3959SLB



Dwg. PP-069-4

Note that the A3959SLB(SOIC) and A3959SB (DIP) do not share a common terminal assignment.

ABSOLUTE MAXIMUM RATINGS

Load Supply Voltage, V_{BB} ..... **50 V**
Output Current, I_{OUT} (Repetitive) ..... **±3.0 A**
(Peak, <3 µs) ..... **±6.0 A**
Logic Supply Voltage, V_{DD} ..... **7.0 V**
Logic Input Voltage Range, V_{IN}
(Continuous) ..... **-0.3 V to V_{DD} + 0.3 V**
(t_w <30 ns) ..... **-1.0 V to V_{DD} + 1.0 V**
Sense Voltage, V_S (Continuous) ..... **0.5 V**
(t_w <3 µs) ..... **2.5 V**
Reference Voltage, V_{REF} ..... **V_{DD}**
Package Power Dissipation (T_A = 25°C), P_D
A3959SB ..... **3.1 W***
A3959SLB ..... **1.6 W***
Operating Temp. Range, T_A .... **-20°C to +85°C**
Junction Temperature, T_J ..... **+150°C**
Storage Temp. Range, T_S ..... **-55°C to +150°C**

Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.

* Per SEMI G42-88 Specification.

Designed for pulse-width modulated (PWM) current control of dc motors, the A3959SB and A3959SLB are capable of output currents to ±3 A and operating voltages to 50 V. Internal fixed off-time PWM current-control timing circuitry can be adjusted via control inputs to operate in slow, fast, and mixed current-decay modes.

PHASE and ENABLE input terminals are provided for use in controlling the speed and direction of a dc motor with externally applied PWM-control signals. Internal synchronous rectification control circuitry is provided to reduce power dissipation during PWM operation.

Internal circuit protection includes thermal shutdown with hysteresis, undervoltage monitoring of supply and charge pump, and crossover-current protection. Special power-up sequencing is not required.

The A3959SB/SLB is supplied in a choice of two power packages, a 24-pin plastic DIP with a copper batwing tab (package suffix 'B'), and a 24-lead plastic SOIC with a copper batwing tab (package suffix 'LB'). In both cases, the power tab is at ground potential and needs no electrical isolation.

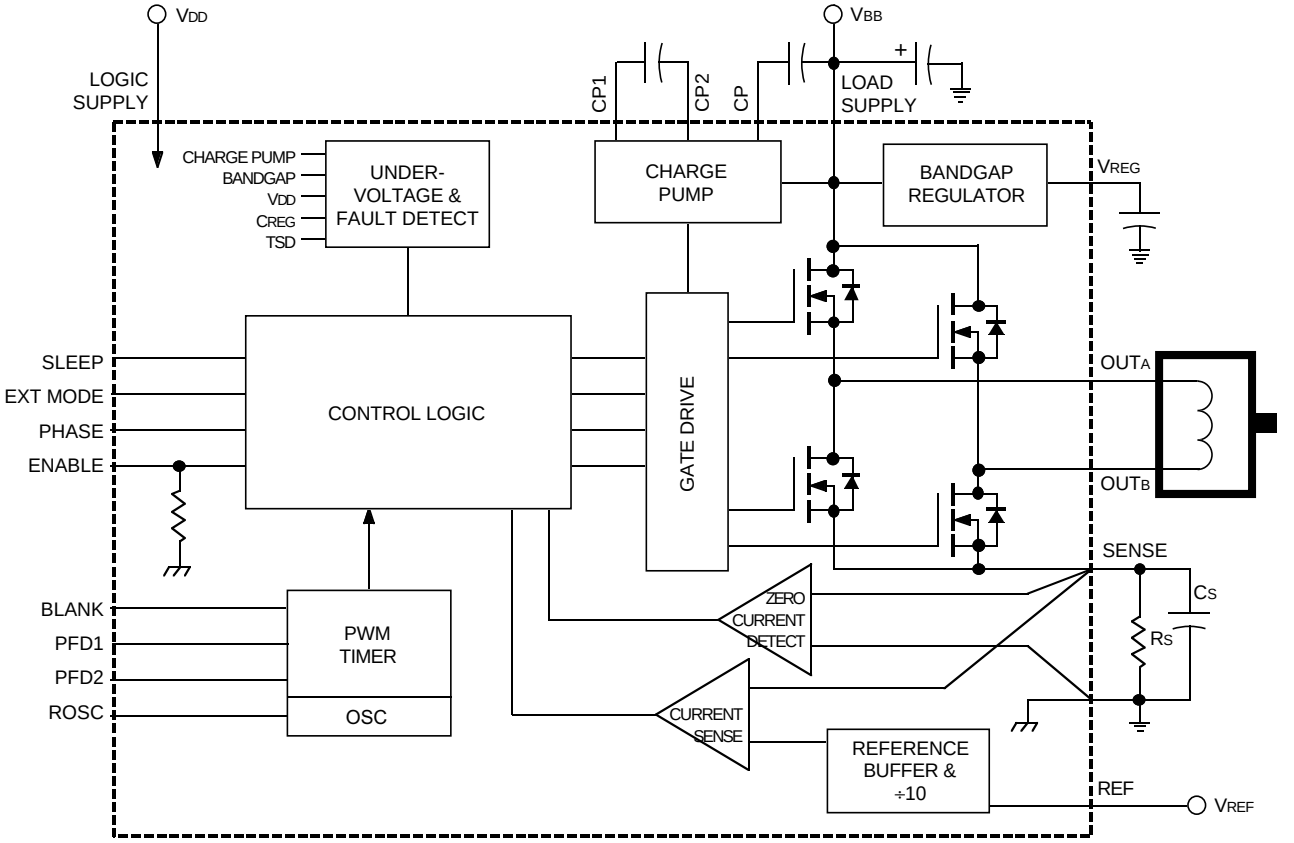
FEATURES

- ±3 A, 50 V Output Rating
- Low $r_{DS(on)}$ Outputs (270 mΩ, Typical)
- Mixed, Fast, and Slow Current-Decay Modes
- Synchronous Rectification for Low Power Dissipation
- Internal UVLO and Thermal-Shutdown Circuitry
- Crossover-Current Protection
- Internal Oscillator for Digital PWM Timing

Always order by complete part number:

Part Number	Package	$R_{\theta JA}$	$R_{\theta JT}$
A3959SB	24-pin batwing DIP	40°C/W	6°C/W
A3959SLB	24-lead batwing SOIC	77°C/W	6°C/W

FUNCTIONAL BLOCK DIAGRAM



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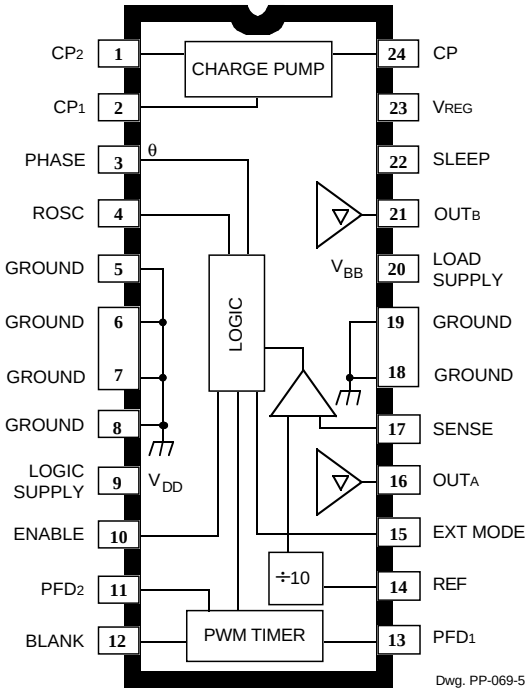

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A3959SB

Note that the A3959SLB (SOIC) and A3959SB (DIP) do not share a common terminal assignment.

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ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 50 V, V_{DD} = 5.0 V, V_{SENSE} = 0.5 V, f_{PWM} < 50 kHz (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Drivers						
Load Supply Voltage Range	V_{BB}	Operating	9.5	–	50	V
		During sleep mode	0	–	50	V
Output Leakage Current	I_{DSS}	V_{OUT} = V_{BB}	–	<1.0	20	µA
		V_{OUT} = 0 V	–	<-1.0	-20	µA
Output On Resistance	$r_{DS(on)}$	Source driver, I_{OUT} = -3 A	–	270	300	mΩ
		Sink driver, I_{OUT} = 3 A	–	270	300	mΩ
Crossover Delay			300	600	1000	ns
Body Diode Forward Voltage	V_F	Source diode, I_F = -3 A	–	–	1.6	V
		Sink diode, I_F = 3 A	–	–	1.6	V
Load Supply Current	I_{BB}	f_{PWM} < 50 kHz	–	4.0	7.0	mA
		Charge pump on, outputs disabled	–	2.0	5.0	mA
		Sleep Mode	–	–	20	µA
Control Logic						
Logic Supply Voltage Range	V_{DD}	Operating	4.5	5.0	5.5	V
Logic Input Voltage	$V_{IN(1)}$		2.0	–	–	V
	$V_{IN(0)}$		–	–	0.8	V
Logic Input Current (all inputs except ENABLE)	$I_{IN(1)}$	V_{IN} = 2.0 V	-20	<1.0	20	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	–	<-2.0	-20	µA
ENABLE Input Current	$I_{IN(1)}$	V_{IN} = 2.0 V	–	40	100	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	–	16	40	µA
Internal OSC frequency	f_{OSC}	R_{OSC} shorted to GROUND	3.0	4.0	5.0	MHz
		R_{OSC} = 51 kΩ	3.4	4.0	4.6	MHz
Reference Input Volt. Range	V_{REF}	Operating	0.0	–	V_{DD}	V
Reference Input Current	I_{REF}	V_{REF} = V_{DD}	–	–	±1.0	µA
Comparator Input Offset Volt.	V_{IO}	V_{REF} = 0 V	–	±5.0	–	mV

Continued next page …

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 50 V, V_{DD} = 5.0 V, V_{SENSE} = 0.5 V, f_{PWM} < 50 kHz (unless noted otherwise), continued.

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Control Logic						
Reference Divider Ratio	–		–	10	–	–
G_m Error	E_{Gm}	V_{REF} = V_{DD}	–	–	±4.0	%
(Note 3)		V_{REF} = 0.5 V	–	–	±14	%
Propagation Delay Times	t_{pd}	0.5 E_{in} to 0.9 E_{out}:				
		PWM change to source on	600	750	1000	ns
		PWM change to source off	50	150	350	ns
		PWM change to sink on	600	750	1000	ns
		PWM change to sink off	50	100	150	ns
Thermal Shutdown Temp.	T_J		–	165	–	°C
Thermal Shutdown Hysteresis	ΔT_J		–	15	–	°C
UVLO Enable Threshold	UVLO	Increasing V_{DD}	3.90	4.2	4.45	V
UVLO Hysteresis	ΔUVLO		0.05	0.10	–	V
Logic Supply Current	I_{DD}	f_{PWM} < 50 kHz	–	6.0	10	mA
		Sleep Mode	–	–	2.0	mA

NOTES: 1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device terminal.
3. G_m error = $([V_{REF}/10] – V_{SENSE})/(V_{REF}/10)$ where $V_{SENSE} = I_{TRIP} \cdot R_S$.

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FUNCTIONAL DESCRIPTION

V_{REG}. This internally generated voltage is used to operate the sink-side DMOS outputs. The V_{REG} terminal should be decoupled with a 0.22 µF capacitor to ground. V_{REG} is internally monitored and in the case of a fault condition, the outputs of the device are disabled.

Charge Pump. The charge pump is used to generate a gate-supply voltage greater than V_{BB} to drive the source-side DMOS gates. A 0.22 µF ceramic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.22 µF ceramic capacitor should be connected between CP and V_{BB} to act as a reservoir to operate the high-side DMOS devices. The CP voltage is internally monitored and, in the case of a fault condition, the source outputs of the device are disabled.

PHASE Logic. The PHASE input terminal determines if the device is operating in the "forward" or "reverse" state.

PHASE	OUT_A	OUT_B
0	Low	High
1	High	Low

ENABLE Logic. The ENABLE input terminal allows external PWM. ENABLE high turns on the selected sink-source pair. ENABLE low switches off the source driver or the source and sink driver, depending on EXT MODE, and the load current decays. If ENABLE is kept high, the current will rise until it reaches the level set by the internal current-control circuit.

ENABLE	Outputs
0	Chopped
1	On

EXT MODE Logic. When using external PWM current control, the EXT MODE input determines the current path during the chopped cycle. With EXT MODE low, fast decay mode, the opposite pair of selected outputs will be enabled during the off cycle. With EXT MODE high, slow decay mode, both sink drivers are on with ENABLE low.

EXT MODE	Decay
0	Fast
1	Slow

Current Regulation. Load current is regulated by an internal fixed off-time PWM control circuit. When the outputs of the DMOS H bridge are turned on, the current increases in the motor winding until it reaches a trip value determined by the external sense resistor (R_S) and the applied analog reference voltage (V_{REF}):

$$I_{TRIP} = V_{REF}/10R_S$$

At the trip point, the sense comparator resets the source-enable latch, turning off the source driver. The load inductance then causes the current to recirculate for the fixed off-time period. The current path during recirculation is determined by the configuration of slow/mixed/fast current-decay mode via PFD1 and PFD2.

Oscillator. The PWM timer is based on an internal oscillator set by a resistor connected from the R_{OSC} terminal to V_{DD}. Typical value of 4 MHz is set with a 51 kΩ resistor. The allowable range of the resistor is from 20 kΩ to 100 kΩ.

$$f_{OSC} = 204 \times 10^9/R_{OSC}.$$

If R_{OSC} is not pulled up to V_{DD}, it must be shorted to ground.

Fixed Off Time. The A3959 is set for a fixed off time of 96 cycles of the internal oscillator, typically 24 µs with a 4 MHz oscillator.

FUNCTIONAL DESCRIPTION (continued)

Internal Current-Control Mode. Inputs PFD1 and PFD2 determine the current-decay method after an overcurrent event is detected at the SENSE input. In slow-decay mode, both sink drivers are turned on for the fixed off-time period. Mixed-decay mode starts out in fast-decay mode for a portion (15% or 48%) of the fixed off time, and then is followed by slow decay for the remainder of the period.

PFD1	PFD2	% t_{off}	Decay
0	0	0	Slow
0	1	15	Mixed
1	0	48	Mixed
1	1	100	Fast

PWM Blank Timer. When a source driver turns on, a current spike occurs due to the reverse-recovery currents of the clamp diodes and/or switching transients related to distributed capacitance in the load. To prevent this current spike from erroneously resetting the source-enable latch, the sense comparator is blanked. The blank timer runs after the off-time counter to provide the blanking function. The blank timer is reset when ENABLE is chopped or PHASE is changed. For external PWM control, a PHASE change or ENABLE on will trigger the blanking function. The duration is determined by the BLANK input and the oscilator.

BLANK	t_{blank}
0	$6/f_{osc}$
1	$12/f_{osc}$

Synchronous Rectification. When a PWM off cycle is triggered, either by an ENABLE chop command or internal fixed off-time cycle, load current will recirculate according to the decay mode selected by the control logic. The A3959 synchronous rectification feature will turn on the appropriate pair of DMOS outputs during the current decay and effectively short out the body diodes with the low $r_{DS(on)}$ driver. This will reduce power dissipation significantly and can eliminate the need for external Schottky diodes.

Synchronous rectification will prevent reversal of load current by turning off all outputs when a zero-current level is detected.

Shutdown. In the event of a fault (excessive junction temperature, or low voltage on CP or V_{REG}) the outputs of the device are disabled until the fault condition is removed. At power up, and in the event of low V_{DD}, the UVLO circuit disables the drivers.

Braking. The braking function is implemented by driving the device in slow-decay mode via EXTMODE and applying an enable chop command. Because it is possible to drive current in either direction through the DMOS drivers, this configuration effectively shorts out the motor-generated BEMF as long as the ENABLE chop mode is asserted. It is important to note that the internal PWM current-control circuit will not limit the current when braking, because the current does not flow through the sense resistor. The maximum brake current can be approximated by V_{BEMF}/R_L. Care should be taken to ensure that the maximum ratings of the device are not exceeded in worst-case braking situations of high speed and high inertial loads.

SLEEP Logic. The SLEEP input terminal is used to minimize power consumption when when not in use. This disables much of the internal circuitry including the regulator and charge pump. Logic low will put the device into sleep mode, logic high will allow normal operation.

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FUNCTIONAL DESCRIPTION (continued)

Current Sensing. To minimize inaccuracies in sensing the I_{TRIP} current level, which may be caused by ground trace IR drops, the sense resistor should have an independent ground return to the ground terminal of the device. For low-value sense resistors the IR drops in the PCB sense resistor's traces can be significant and should be taken into account. The use of sockets should be avoided as they can introduce variation in R_S due to their contact resistance.

The maximum value of R_S is given as $R_S \le 0.5/I_{TRIP}$ where $I_{TRIP} \le 3.0$ A.

Thermal Protection. Circuitry turns off all drivers when the junction temperature reaches 165°C typically. It is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. Thermal shutdown has a hysteresis of approximately 15°C.

Layout. The printed wiring board should use a heavy ground plane. For optimum electrical and thermal performance*, the driver should be soldered directly onto the board. The ground side of R_S should have an individual path to the ground terminals of the device. This path should be as short as is possible physically and should not have any other components connected to it. It is recommended that a 0.1 µF capacitor be placed between SENSE and ground as close to the device as possible; the load supply terminal, V_{BB}, should be decoupled with an electrolytic capacitor (> 47 µF is recommended) placed as close to the device as is possible.

* The thermal resistance and absolute maximum allowable package power dissipation specified on page 1 is measured on typical two-sided PCB with minimal copper ground area. See also, Application Note 29501.5, *Improving Batwing Power Dissipation*.

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Terminal List

Terminal Name	Terminal Description	A3959SLB (SOIC)	A3959SB (DIP)
CP	Reservoir capacitor (typically 0.22 µF)	1	24
CP1 & CP2	The charge pump capacitor (typically 0.22 µF)	2 & 3	1 & 2
PHASE	Logic input for direction control	4	3
ROSC	Oscillator resistor	5	4
GROUND	Grounds	6, 7	5, 6, 7, 8*
LOGIC SUPPLY	V_{DD}, the low voltage (typically 5 V) supply	8	9
ENABLE	Logic input for enable control	9	10
PFD2	Logic-level input for fast decay	10	11
BLANK	Logic-level input for blanking control	11	12
PFD1	Logic-level input for fast decay	12	13
REF	V_{REF}, the load current reference input voltage	13	14
EXT MODE	Logic input for PWM mode control	14	15
NO CONNECT	No (Internal) Connection	15	—
OUT_A	One of two DMOS bridge outputs to the motor	16	16
SENSE	Sense resistor	17	17
GROUND	Grounds	18, 19	18, 19*
LOAD SUPPLY	V_{BB}, the high-current, 9.5 V to 50 V, motor supply	20	20
OUT_B	One of two DMOS bridge outputs to the motor	21	21
NO CONNECT	No (Internal) connection	22	—
SLEEP	Logic-level Input for sleep operation	23	22
V_{REG}	Regulator decoupling capacitor (typically 0.22 µF)	24	23

* For the A3959SB DIP only, there is an indeterminate resistance between the substrate grounds (pins 6, 7, 18, and 19) and the grounds at pins 5 and 8. Pins 5 and 8, and 6, 7, 18, or 19 must be connected together externally.

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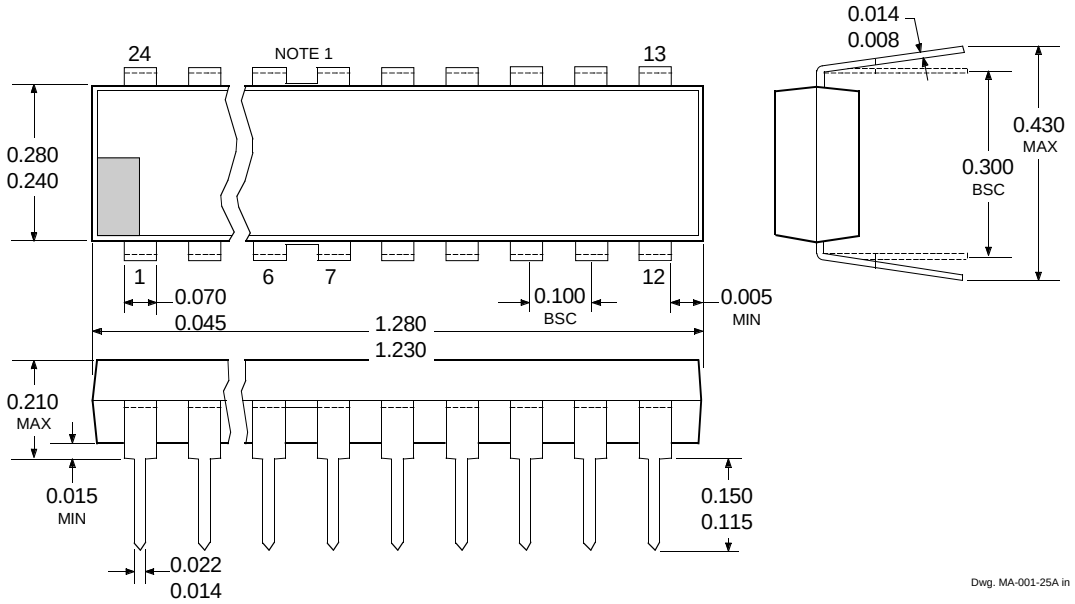
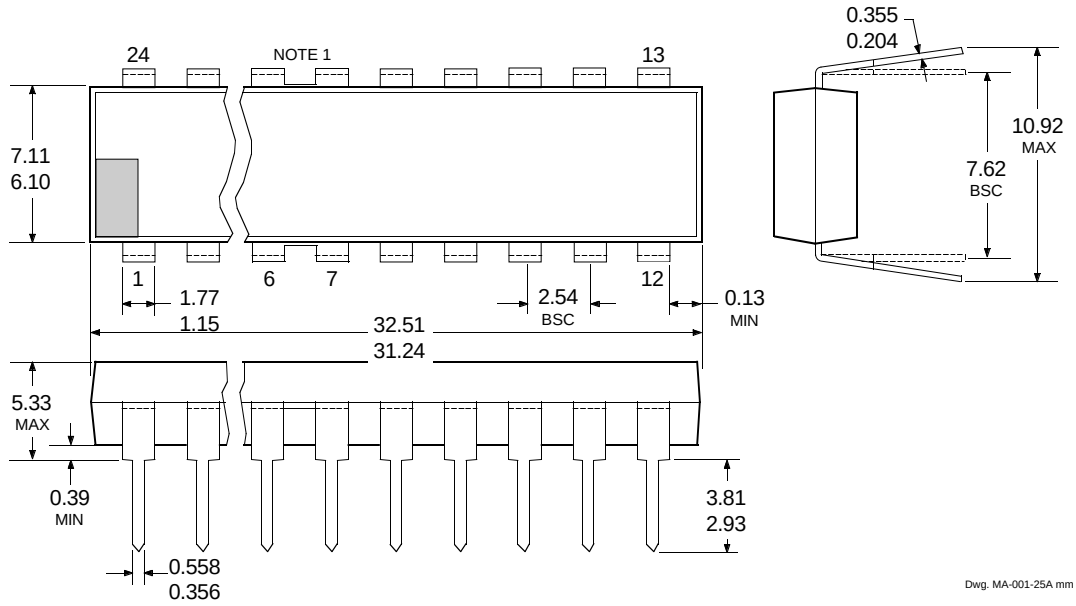
A3959SB

Dimensions in Inches
(controlling dimensions)



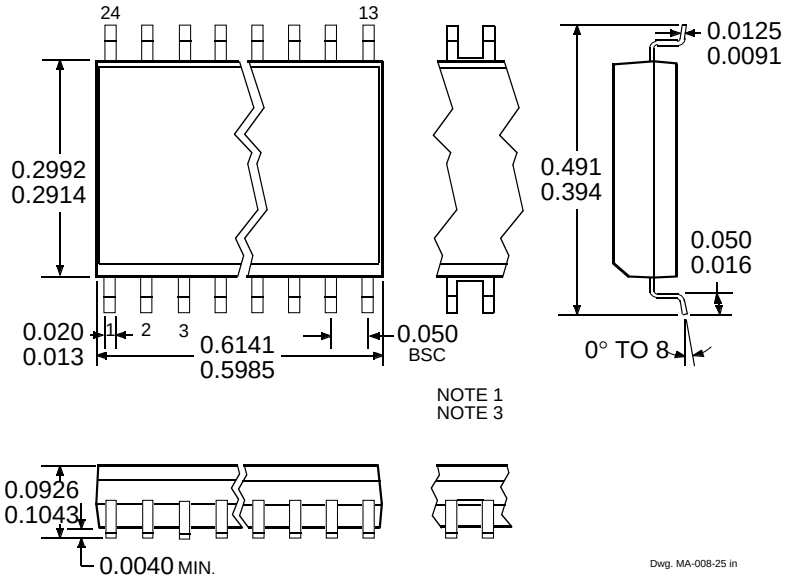
Dimensions in Millimeters
(for reference only)



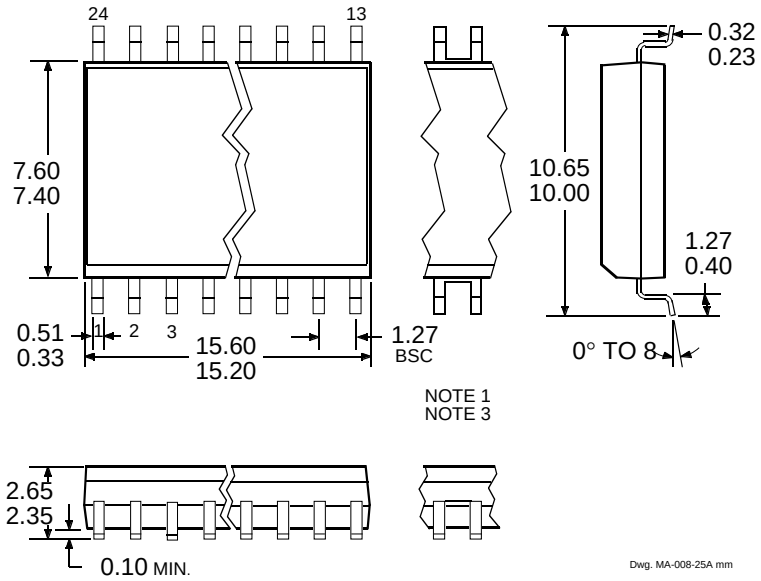
NOTES: 1. Webbed lead frame. Leads 6, 7, 18, and 19 are internally one piece.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead spacing tolerance is non-cumulative.
4. Lead thickness is measured at seating plane or below.
5. Supplied in standard sticks/tubes of 15 devices.

A3959SLB

Dimensions in Inches
(for reference only)



Dimensions in Millimeters
(controlling dimensions)



NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Webbed lead frame. Leads 6, 7, 18, and 19 are internally one piece.
4. Supplied in standard sticks/tubes of 31 devices or add "TR" to part number for tape and reel.

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