FAIRCHILD SEMICONDUCTOR®

October 2013

FDP047AN08A0 / FDH047AN08A0

N-Channel PowerTrench® MOSFET

75 V, 80 A, 4.7 mΩ

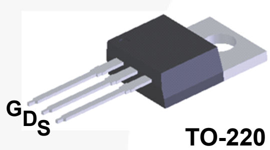
Features

- $R_{DS(ON)}$ = 4.0 mΩ (Typ.), V_{GS} = 10 V, I_D = 80 A
- Q_g(tot) = 92 nC (Typ.), V_{GS} = 10V
- Low Miller Charge
- Low Q_{rr} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)

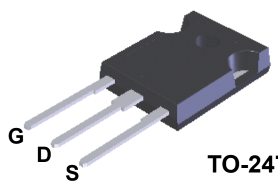
Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies

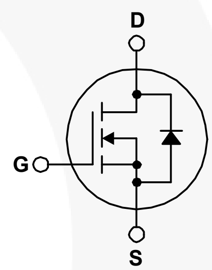
Formerly developmental type 82684



TO-220



TO-247



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	FDP047AN08A0 FDH047AN08A0	Unit
V_{DSS}	Drain to Source Voltage	75	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_C < 144°C, V_{GS} = 10V)	80	A
	Continuous (T_C = 25°C, V_{GS} = 10V, with $R_{\theta JA}$ = 62°C/W)	15	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	475	mJ
P_D	Power dissipation	310	W
	Derate above 25°C	2.0	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case, Max. TO-220, TO-247	0.48	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, Max. TO-220 (Note 2)	62	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, Max. TO-247 (Note 2)	30	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP047AN08A0	FDP047AN08A0	TO-220	Tube	N/A	50 units
FDH047AN08A0	FDH047AN08A0	TO-247	Tube	N/A	30 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit

Off Characteristics

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V		75	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60V		-	-	1	μA
		V_{GS} = 0V	T_C = 150°C	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V		-	-	±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 80A, V_{GS} = 10V	-	0.0040	0.0047	Ω
		I_D = 37A, V_{GS} = 6V	-	0.0058	0.0087	
		I_D = 80A, V_{GS} = 10V, T_J = 175°C	-	0.0082	0.011	

Dynamic Characteristics

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
C_{ISS}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	6600	-	pF
C_{OSS}	Output Capacitance			-	1000	-	pF
C_{RSS}	Reverse Transfer Capacitance			-	240	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V	V_{DD} = 40V, I_D = 80A, I_g = 1.0mA	-	92	138	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 2V		-	11	17	nC
Q_{gs}	Gate to Source Gate Charge			-	27	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau			-	16	-	nC
Q_{gd}	Gate to Drain “Miller” Charge			-	21	-	nC

Switching Characteristics (V_{GS} = 10V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{ON}	Turn-On Time	V_{DD} = 40V, I_D = 80A, V_{GS} = 10V, R_{GS} = 3.3Ω	-	-	160	ns
$t_{d(ON)}$	Turn-On Delay Time		-	18	-	ns
t_r	Rise Time		-	88	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	40	-	ns
t_f	Fall Time		-	45	-	ns
t_{OFF}	Turn-Off Time		-	-	128	ns

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 80A	-	-	1.25	V
		I_{SD} = 40A	-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 75A, dI_{SD}/dt = 100A/μs	-	-	53	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 75A, dI_{SD}/dt = 100A/μs	-	-	54	nC

Notes:
1: Starting T_J = 25°C, L = 0.232mH, I_{AS} = 64A.
2: Pulse Width = 100s

Typical Characteristics T_C = 25°C unless otherwise noted

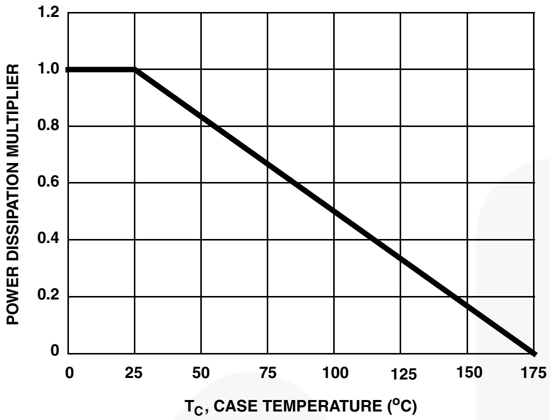


Figure 1. Normalized Power Dissipation vs Case Temperature

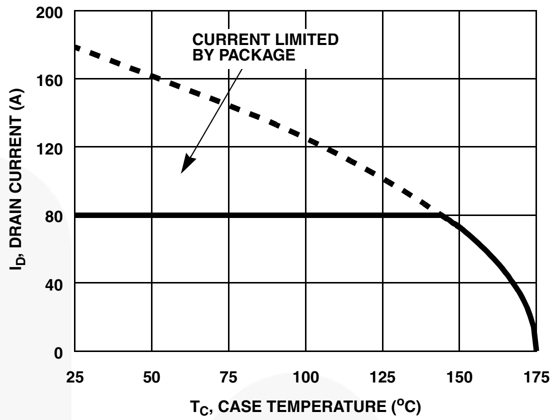


Figure 2. Maximum Continuous Drain Current vs Case Temperature

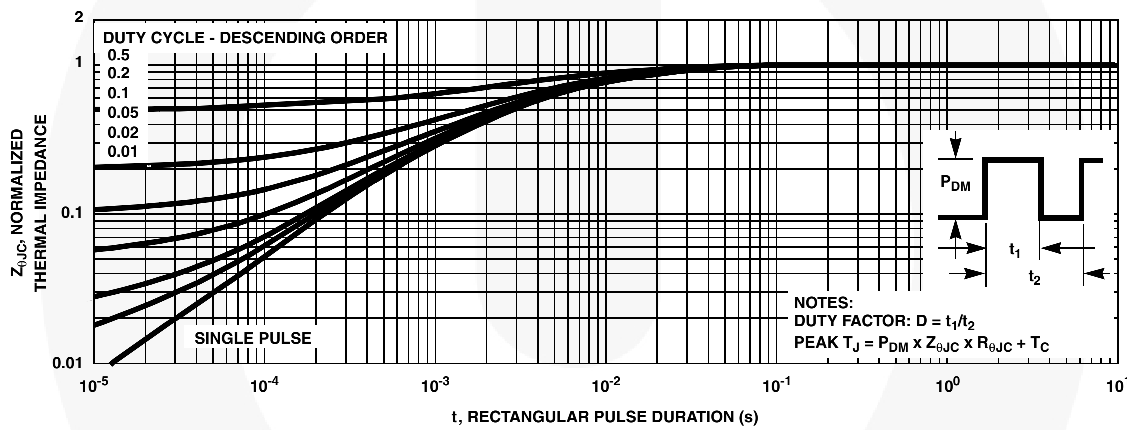


Figure 3. Normalized Maximum Transient Thermal Impedance

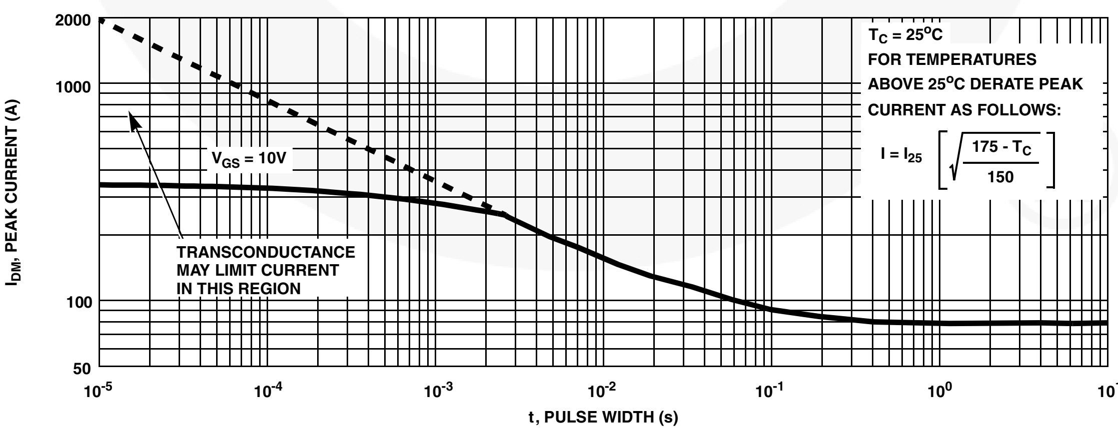


Figure 4. Peak Current Capability

Typical Characteristics $T_C = 25°C$ unless otherwise noted

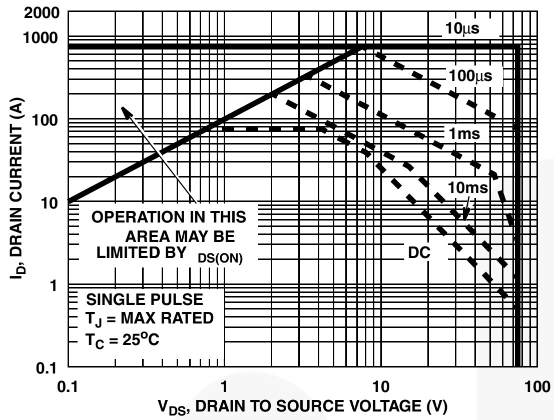
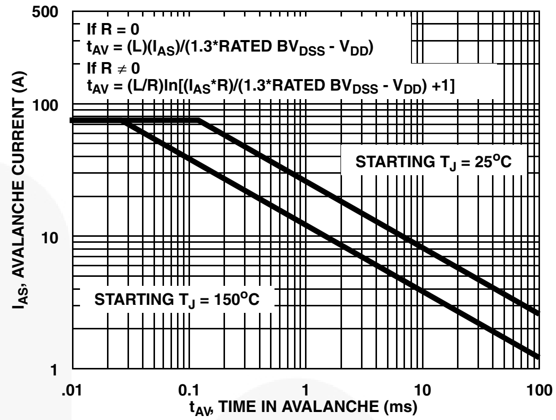


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

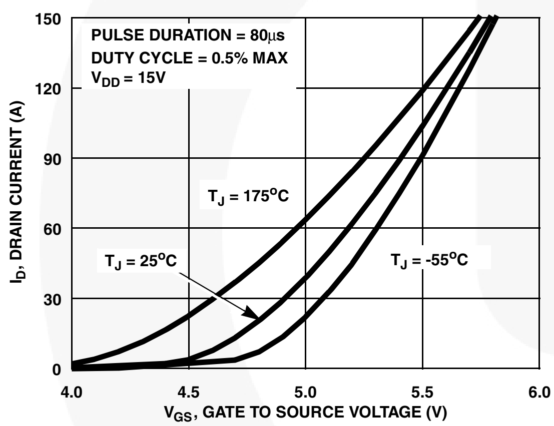


Figure 7. Transfer Characteristics

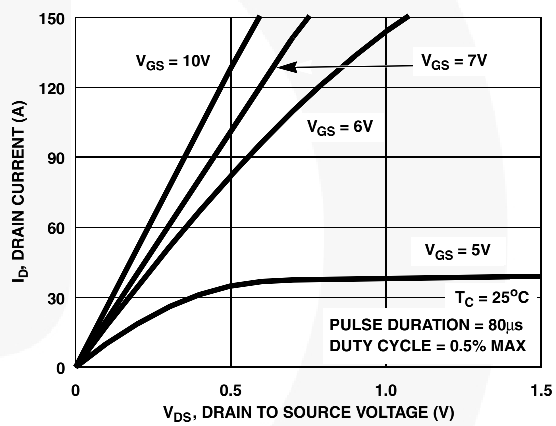


Figure 8. Saturation Characteristics

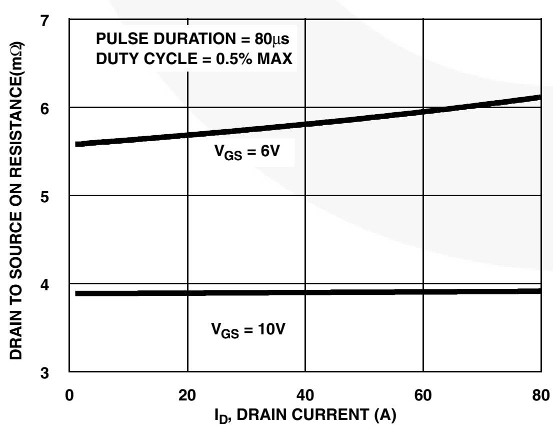


Figure 9. Drain to Source On Resistance vs Drain Current

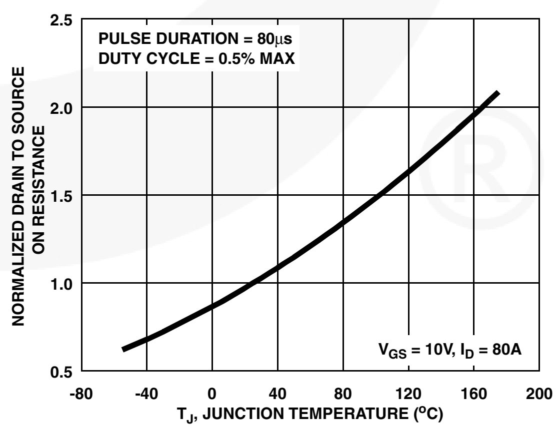


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics T_C = 25°C unless otherwise noted

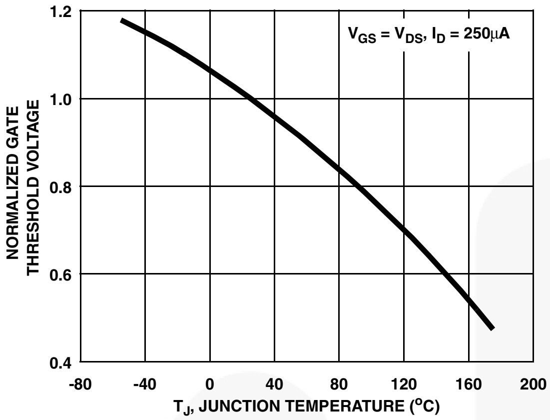


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

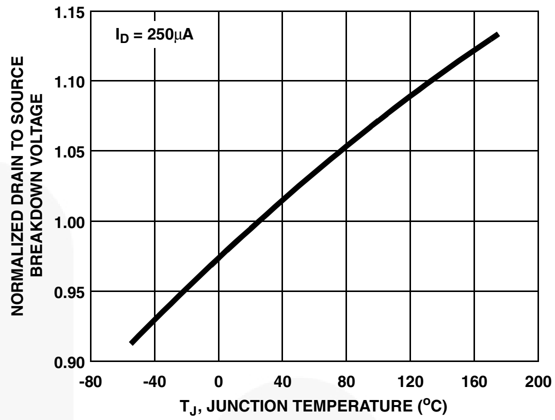


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

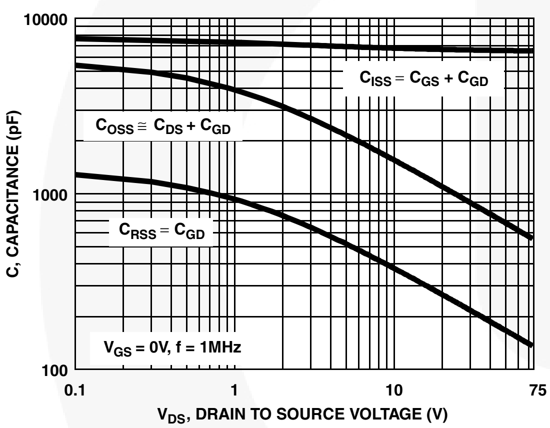


Figure 13. Capacitance vs Drain to Source Voltage

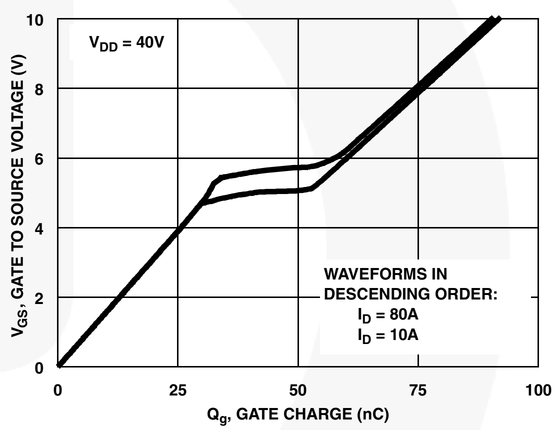


Figure 14. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms

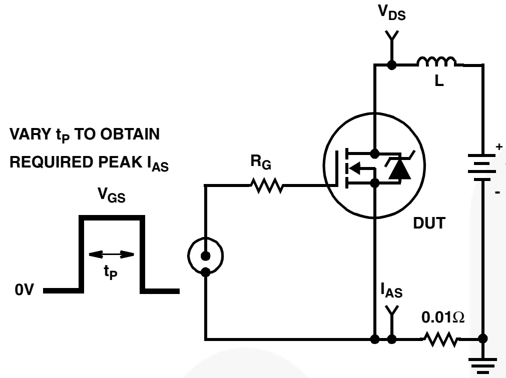


Figure 15. Unclamped Energy Test Circuit

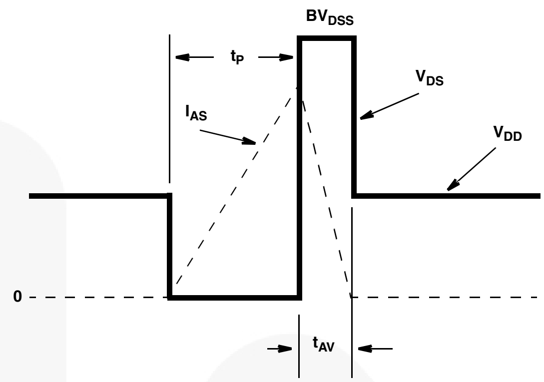


Figure 16. Unclamped Energy Waveforms

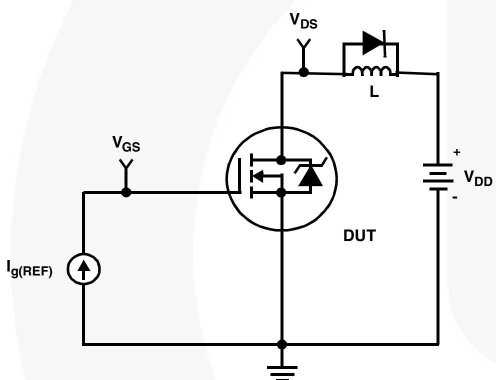


Figure 17. Gate Charge Test Circuit

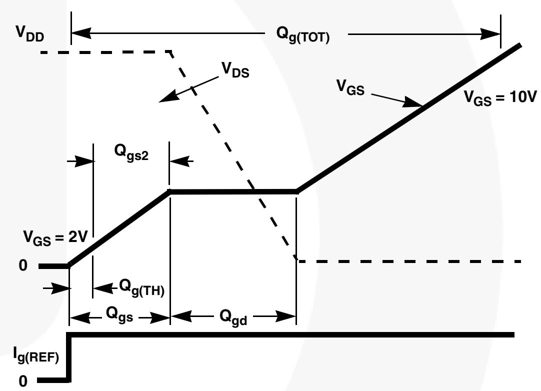


Figure 18. Gate Charge Waveforms

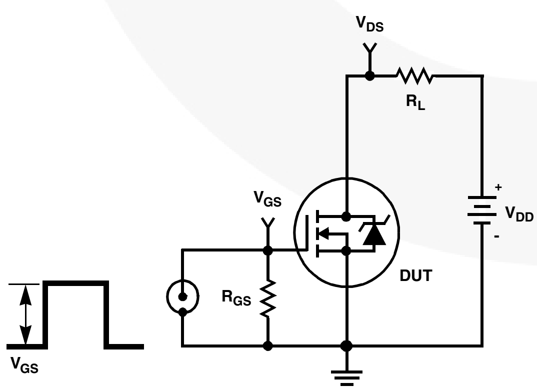


Figure 19. Switching Time Test Circuit

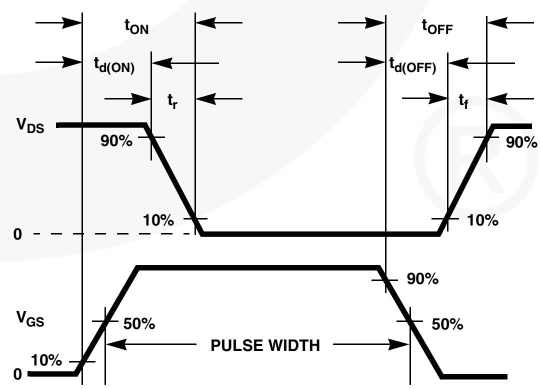
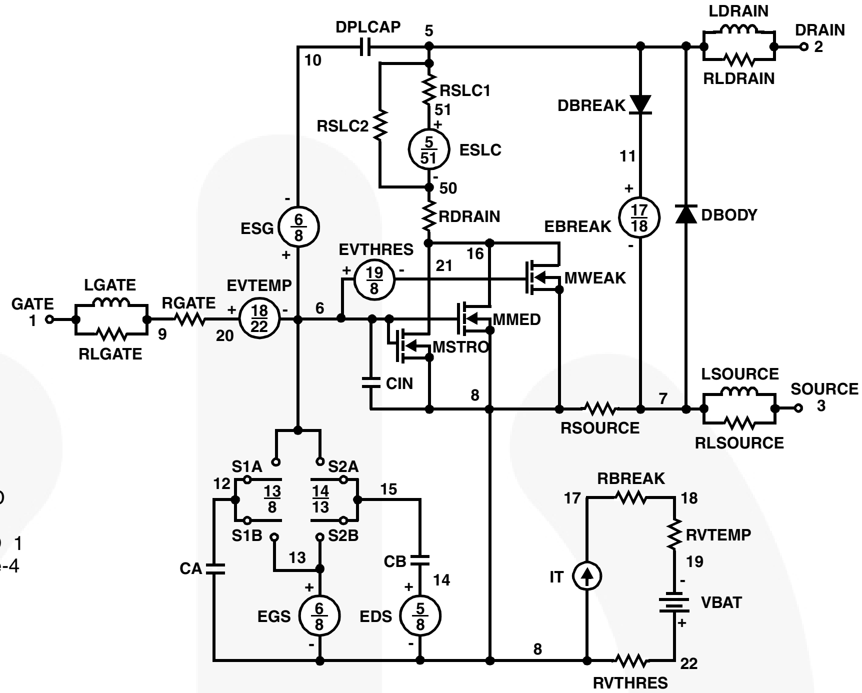


Figure 20. Switching Time Waveforms

PSPICE Electrical Model

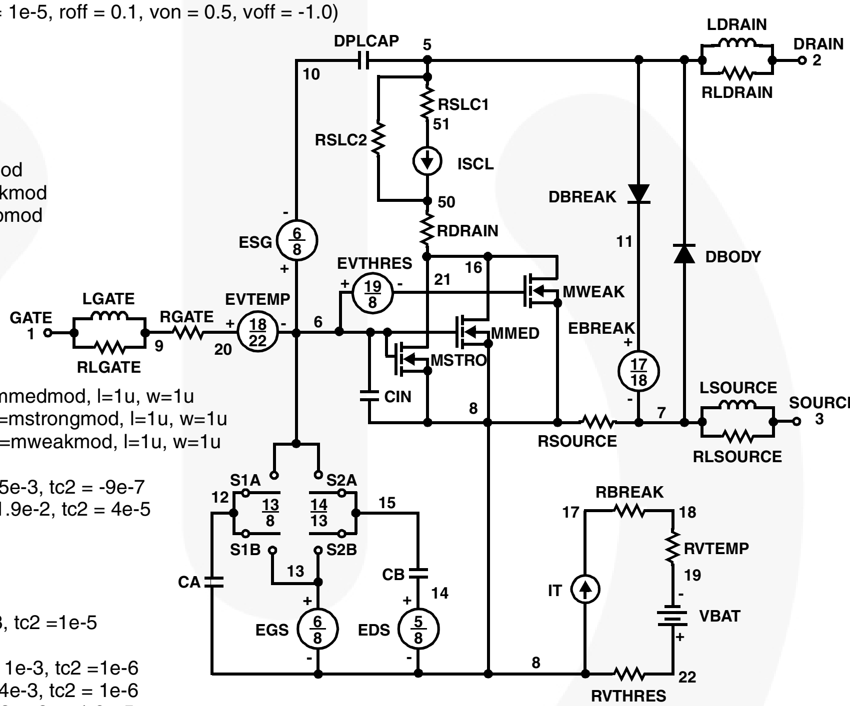



```
.SUBCKT FDP047AN08A0 2 1 3 ;        rev March 2002
CA  12  8 1.5e-9
CB  15  14 1.5e-9
CIN  6  8 6.4e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11  DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17  18 82.3
EDS  14  8  5  8 1
EGS  13  8  6  8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8  1
EVTEMP 20 6 18 22 1

IT  8  17  1

LDRAIN 2 5 1e-9
LGATE 1  9 4.81e-9
LSOURCE  3  7 4.63e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK  17  18  RBREAKMOD  1
RDRAIN 50 16 RDRAINMOD 9e-4
RGATE  9  20 1.36
RLDRAIN 2 5 10
RLGATE 1 9 48.1
RLSOURCE 3 7 46.3
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE  8  7  RSOURCEMOD 2.3e-3
RVTHRES 22 8 RVTHRESMOD  1
RVTEMP 18 19 RVTEMPMOD 1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT 22 19  DC  1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*250),10))}

.MODEL DBODYMOD D (IS = 2.4e-11 N = 1.04  RS = 1.76e-3  TRS1 = 2.7e-3  TRS2 = 2e-7 XTI=3.9  CJO = 4.35e-9  TT = 1e-8
M = 5.4e-1)
.MODEL DBREAKMOD D (RS = 1.5e-1  TRS1 = 1e-3  TRS2 = -8.9e-6)
.MODEL DPLCAPMOD D (CJO = 1.35e-9  IS = 1e-30  N = 10 M = 0.53)
.MODEL MMEDMOD NMOS (VTO = 3.7 KP = 9  IS =1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.36)
.MODEL MSTROMOD NMOS (VTO = 4.4 KP = 250  IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 3.05 KP = 0.03 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.36e1 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.05e-3  TC2 = -9e-7)
.MODEL RDRAINMOD RES (TC1 = 1.9e-2  TC2 = 4e-5)
.MODEL RSLCMOD RES (TC1 = 1.3e-3 TC2 = 1e-5)
.MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)
.MODEL RVTHRESMOD RES (TC1 = -6e-3 TC2 = -1.9e-5)
.MODEL RVTEMPMOD RES (TC1 = -2.4e-3  TC2 = 1e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -4.0  VOFF= -1.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -1.5  VOFF= -4.0)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -1.0  VOFF= 0.5)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 0.5  VOFF= -1.0)

.ENDS
```

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

REV March 2002
template FDP047AN08A0 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod = (isl = 2.4e-11, n1 = 1.04, rs = 1.76e-3, trs1 = 2.7e-3, trs2 = 2e-7, xti = 3.9, cjo = 4.35e-9, tt = 1e-8, m = 5.4e-1)
dp..model dbreakmod = (rs = 1.5e-1, trs1 = 1e-3, trs2 = -8.9e-6)
dp..model dplcapmod = (cjo = 1.35e-9, isl =10e-30, nl =10, m = 0.53)
m..model mmedmod = (type=_n, vto = 3.7, kp = 9, is =1e-30, tox=1)
m..model mstrongmod = (type=_n, vto = 4.4, kp = 250, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 3.05, kp = 0.03, is = 1e-30, tox = 1, rs=0.1)
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -4.0, voff = -1.5)
sw_vcsp..model s1bmod = (ron =1e-5, roff = 0.1, von = -1.5, voff = -4.0)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = -1.0, voff = 0.5)
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0.5, voff = -1.0)



c.ca n12 n8 = 1.5e-9
c.cb n15 n14 = 1.5e-9
c.cin n6 n8 = 6.4e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1e-9
l.lgate n1 n9 = 4.81e-9
l.lsource n3 n7 = 4.63e-9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1 = 1.05e-3, tc2 = -9e-7
res.rdrain n50 n16 = 9e-4, tc1 = 1.9e-2, tc2 = 4e-5
res.rgate n9 n20 = 1.36
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 48.1
res.rlsource n3 n7 = 46.3
res.rslc1 n5 n51= 1e-6, tc1 = 1e-3, tc2 =1e-5
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 2.3e-3, tc1 = 1e-3, tc2 =1e-6
res.rvtemp n18 n19 = 1, tc1 = -2.4e-3, tc2 = 1e-6
res.rvthres n22 n8 = 1, tc1 = -6e-3, tc2 = -1.9e-5

spe.ebreak n11 n7 n17 n18 = 82.3
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/250))** 10))
}
}

SPICE Thermal Model

REV 23 March 2002

FDP047AN08A0T

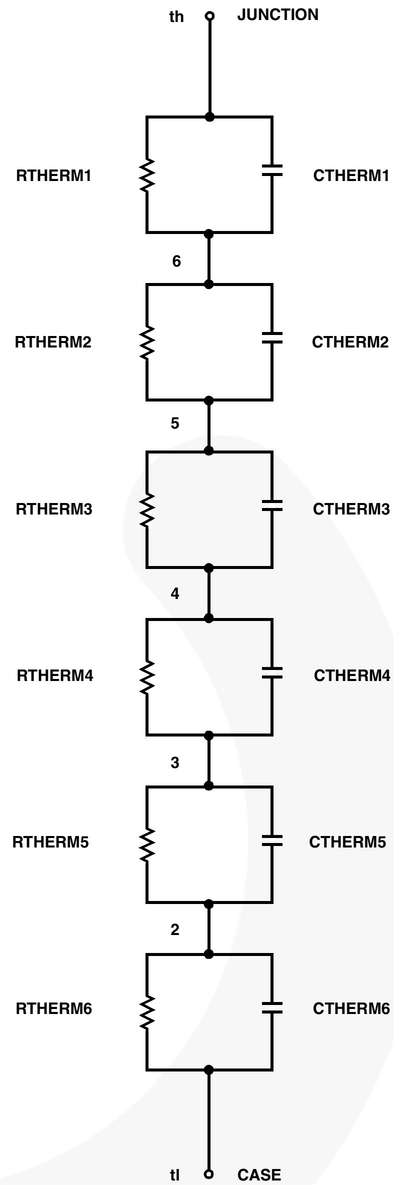
CTHERM1 th 6 6.45e-3
CTHERM2 6 5 3e-2
CTHERM3 5 4 1.4e-2
CTHERM4 4 3 1.65e-2
CTHERM5 3 2 4.85e-2
CTHERM6 2 tl 1e-1

RTHERM1 th 6 3.24e-3
RTHERM2 6 5 8.08e-3
RTHERM3 5 4 2.28e-2
RTHERM4 4 3 1e-1
RTHERM5 3 2 1.1e-1
RTHERM6 2 tl 1.4e-1

SABER Thermal Model

SABER thermal model FDP047AN08A0T
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 6.45e-3
ctherm.ctherm2 6 5 = 3e-2
ctherm.ctherm3 5 4 = 1.4e-2
ctherm.ctherm4 4 3 = 1.65e-2
ctherm.ctherm5 3 2 = 4.85e-2
ctherm.ctherm6 2 tl = 1e-1

rtherm.rtherm1 th 6 = 3.24e-3
rtherm.rtherm2 6 5 = 8.08e-3
rtherm.rtherm3 5 4 = 2.28e-2
rtherm.rtherm4 4 3 = 1e-1
rtherm.rtherm5 3 2 = 1.1e-1
rtherm.rtherm6 2 tl = 1.4e-1
}



Mechanical Dimensions

TO-220 3L

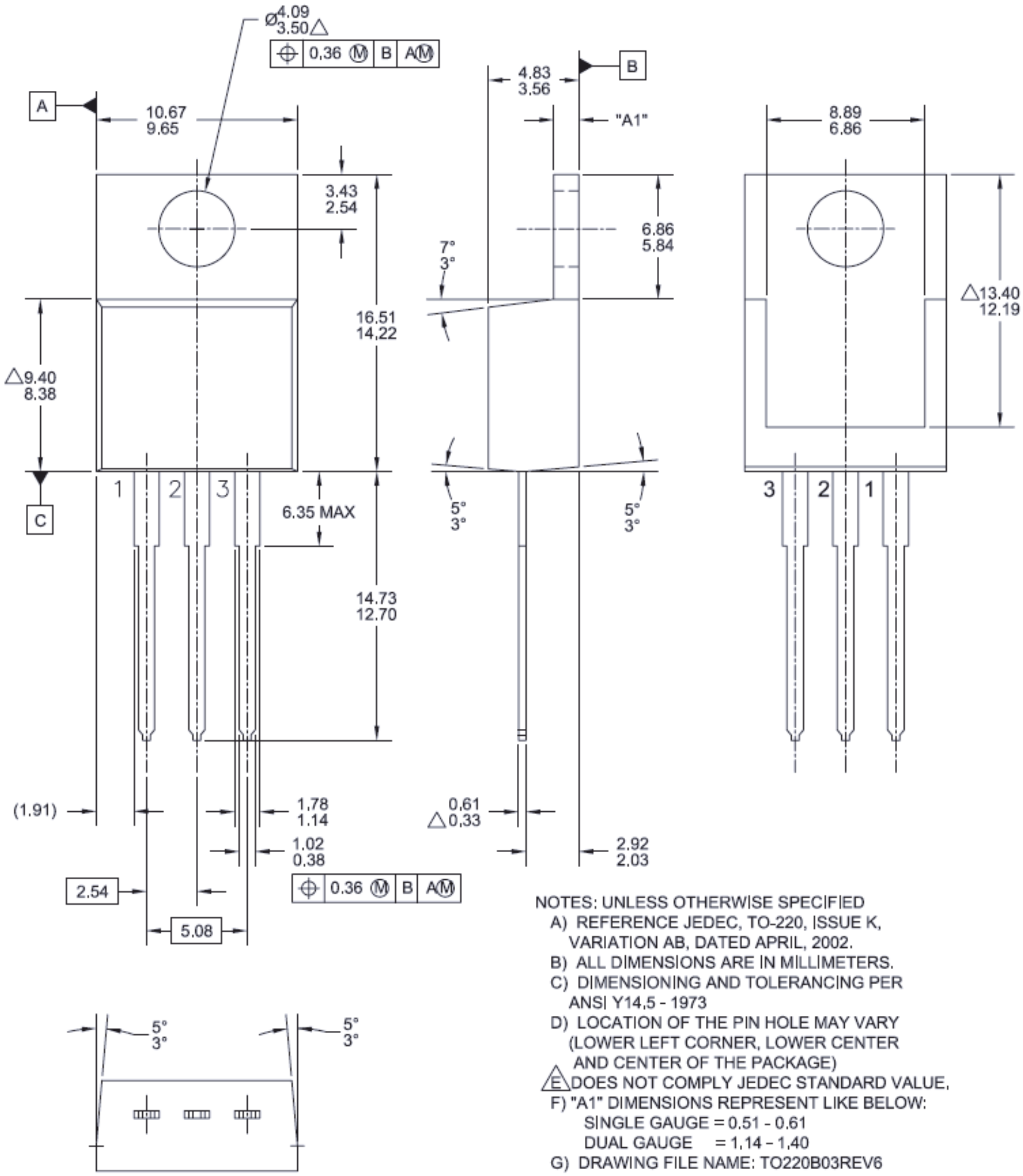


Figure 21. TO-220, Molded, 3Lead, Jedec Variation AB

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

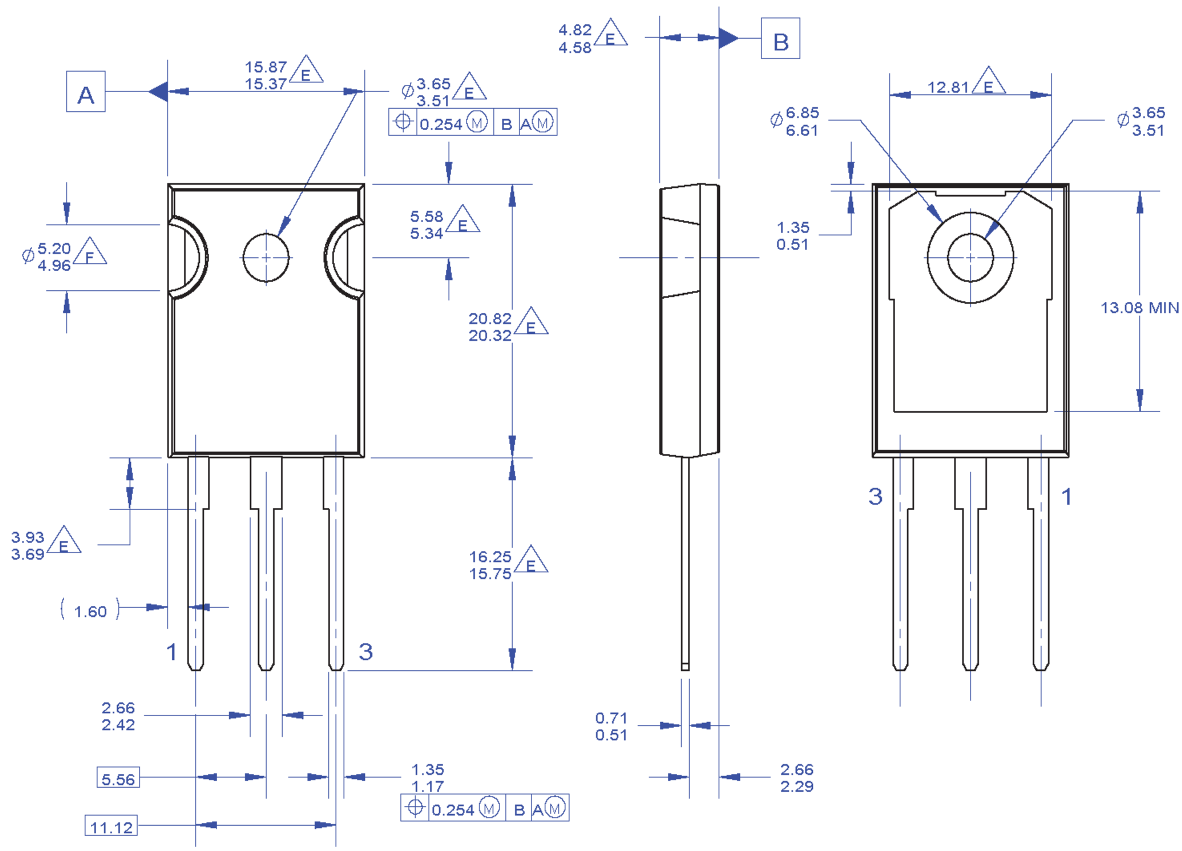
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/package/packageDetails.html?id=PN_TT220-003

Dimension in Millimeters

Mechanical Dimensions

TO-247 3L



NOTES: UNLESS OTHERWISE SPECIFIED.

A. PACKAGE REFERENCE: JEDEC TO-247, ISSUE E, VARIATION AB, DATED JUNE, 2004.
B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DRAWING CONFORMS TO ASME Y14.5 - 1994

E. DOES NOT COMPLY JEDEC STANDARD VALUE

F. NOTCH MAY BE SQUARE

G. DRAWING FILENAME: MKT-TO247A03_REV03

Figure 22. TO-247, Molded, 3 Lead, Jedec Variation AB

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/package/packageDetails.html?id=PN_TO247-003

Dimension in Millimeters

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™
AX-CAP®*
BitSiC™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficentMax™
ESBC™
®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FPS™
F-PFS™
FRFET®
Global Power Resource^SM
GreenBridge™
Green FPS™
Green FPS™ e-Series™
G*max*™
GTO™
IntelliMAX™
ISOPLANAR™
Marking Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
mWSaver®
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®
®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
TinyBoost®
TinyBuck®
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
µSerDes™
SerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™

*Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used here in:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.Fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handing and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I66