# TYN612

## SCRs

**HAOPIN MICROELECTRONICS CO.,LTD.**

### Description

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

| Symbol | Simplified outline |
|---|---|
|   |   TO-220 |

| Pin | Description |
|---|---|
| 1 | Cathode |
| 2 | Anode |
| 3 | Gate |

### Applications:

- Motor control
- Industrial and domestic lighting
- Heating
- Static switching

### Features

- Blocking voltage to 600 V
- On-state RMS current to 12A
- Ultra low gate trigger current

| SYMBOL | PARAMETER | Value | Unit |
|---|---|---|---|
| $V_{DRM}$ | Repetitive peak off-state voltages | 600 | V |
| $I_{T\ (RMS)}$ | RMS on-state current | 12 | A |
| $I_{TSM}$ | Non-repetitive surge peak on-state current | 140 | A |

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Rth( j-c) | Junction to case(DC) | | - | 1.3 | - | ℃/W |
| Rth( j-a) | Junction to ambient | | - | 60 | - | ℃/W |

Limiting values in accordance with the Maximum system(IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | | | MIN | Value | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{DRM}/V_{RRM}$ | | | | | - | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | 180°C conduction angle Tc=105℃ | | | - | 12 | A |
| $I_{TSM}$ | Non repetitive surge peak on-statecurrent | | Tj=25°C | tp=8.3ms | - | -<br>146 | A |
| | | | Tj=25°C | tp=10ms | - | 140 | A |
| $IT_{(AV)}$ | Average on-state current | 180°C conduction angle Tc=105℃ | | | - | - | A |
| $I^2t$ | $I^2t$ Value for fusing | $T_p$=10ms | | Tj=25℃ | - | 98 | $A^2S$ |
| DI/dt | Critical rate of rise of on-state current | IG=2x $I_{GT}$,tr<=100ns | F=60$H_z$ | Tj=125℃ | - | 50 | A/μs |
| $I_{GM}$ | Peak gate current | | tp=20us | Tj=125℃ | - | 4 | A |
| $I_{DRM}$ | $V_{DRM}$=$V_{RRM}$ | | | Tj=25℃ | - | 5 | μA |
| $I_{RRM}$ | $V_{DRM}$=$V_{RRM}$ | | | Tj=125℃ | - | 2 | mA |
| $P_{G(AV)}$ | Average gate power dissipation | | | Tj=125℃ | - | 1 | W |
| $T_{stg}$ | Storage junction temperature range | | | | -40 | 150 | ℃ |
| $T_j$ | Operating junction Temperature range | | | | -40 | 125 | ℃ |

$T_J$=25°C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Static characteristics | | | | | | |
| $I_{GT}$<br>$V_{GT}$ | | $V_D$=12V; RL=33Ω | 2 | - | 15<br>1.3 | mA<br>V |
| $I_L$ | | $I_G$=1.2$I_{GT}$ | - | - | 60 | mA |
| $I_H$ | | $I_T$=500mA Gate open | - | - | 30 | mA |
| $V_{GD}$ | | $V_D$=$V_{DRM}$ $R_L$=3.3KΩ Tj=125℃ | 0.2 | - | - | V |
| dV/dt | | $V_D$=67%$V_{DRM}$ Gateopen;$T_J$=125℃ | 200 | - | - | V/us |

Dynamic Characteristics

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{TM}$ | $I_{TM}$=24A tp=380μs | $T_J$=25℃ | - | - | 1.6 | V |
| $V_{to}$<br>$R_d$ | Threshold voltage<br>Dynamic resistance | $T_J$=125℃<br>$T_J$=125℃ | - | - | 0.85<br>30 | V<br>mΩ |

## Description

**Fig. 1:** Maximum average power dissipation versus average on-state current.

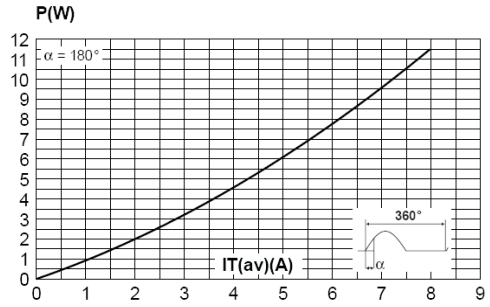



**Fig. 2-1:** Average and D.C. on-state current versus case temperature.

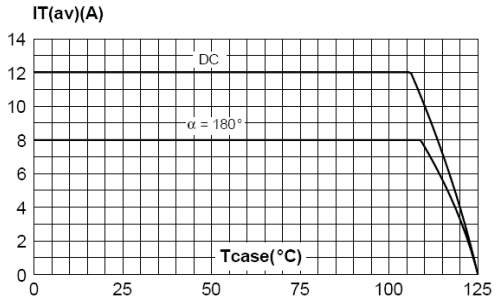



**Fig. 2-2:** Average and D.C. on-state current versus ambient temperature (device mounted on FR4 with recommended pad layout) (DPAK and $D^2PAK$).

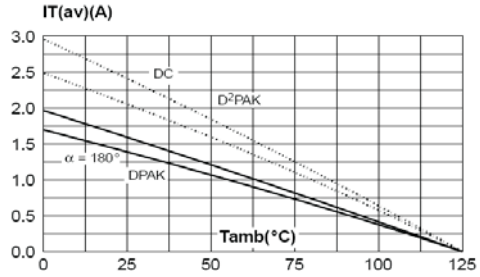



**Fig. 3-1:** Relative variation of thermal impedance junction to case versus pulse duration.

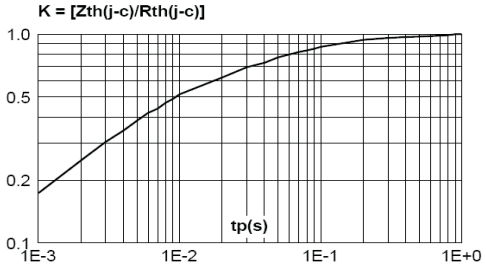



**Fig. 3-2:** Relative variation of thermal impedance junction to ambient versus pulse duration (recommended pad layout, FR4 PC board).

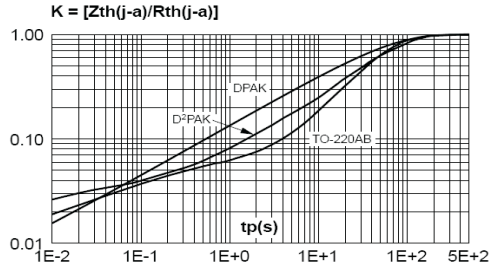
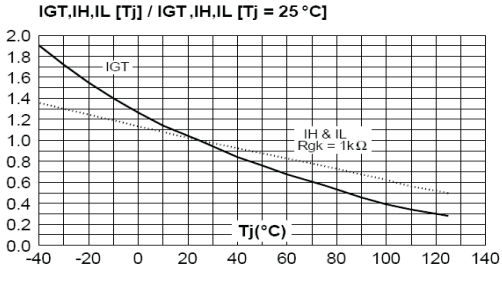



**Fig. 4-1:** Relative variation of gate trigger current, holding current and latching versus junction temperature for TS12 series.



## Description

**Fig. 4-2:** Relative variation of gate trigger current, holding current and latching current versus junction temperature for TN12 & TYN series.

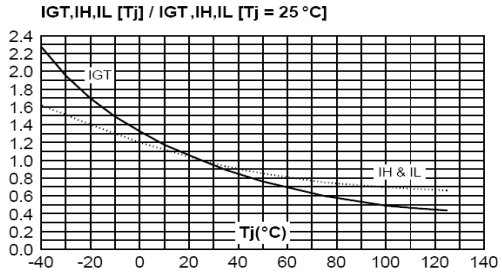



**Fig. 5:** Relative variation of holding current versus gate-cathode resistance (typical values) for TS12 series.

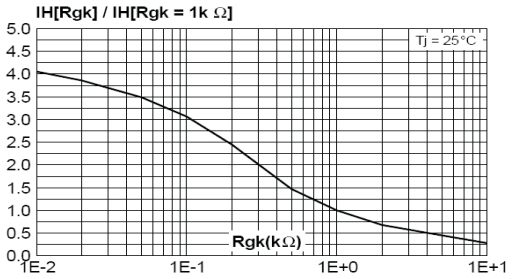



**Fig. 6:** Relative variation of dV/dt immunity versus gate-cathode resistance (typical values) for TS12 series.

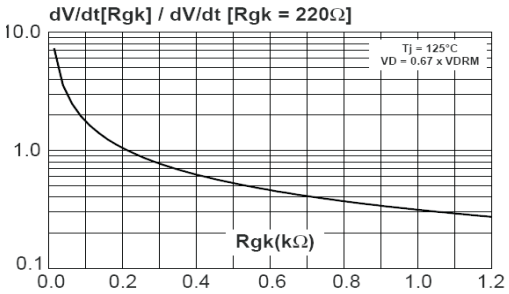



**Fig. 7:** Relative variation of dV/dt immunity versus gate-cathode capacitance (typical values) for TS12 series.

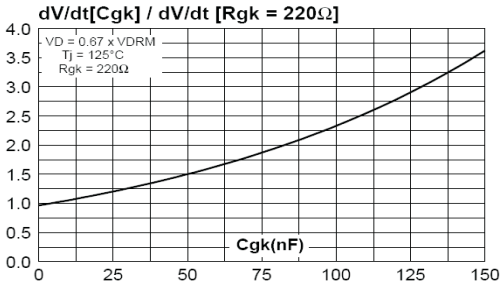



**Fig. 8:** Surge peak on-state current versus number of cycles (TS12/TN12/TYN).

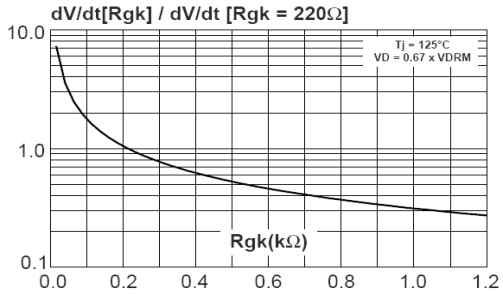
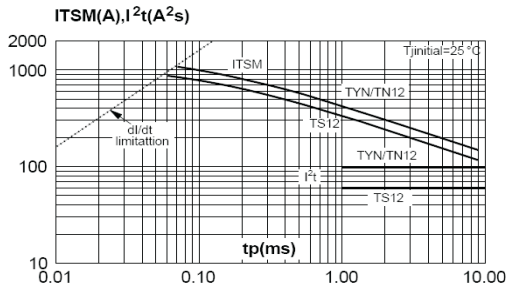



**Fig. 9:** Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp < 10 ms, and corresponding values of $I^2t$.



## Description

**Fig. 10:** On-state characteristics (maximum values).

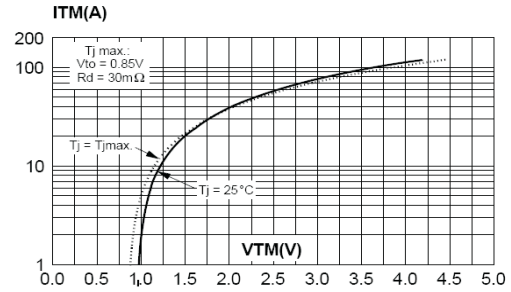
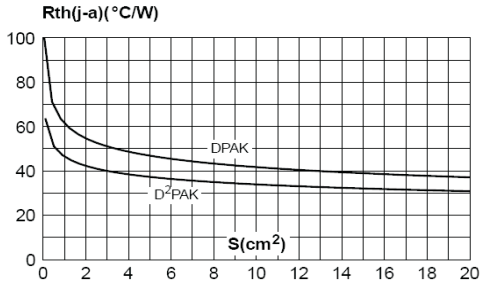


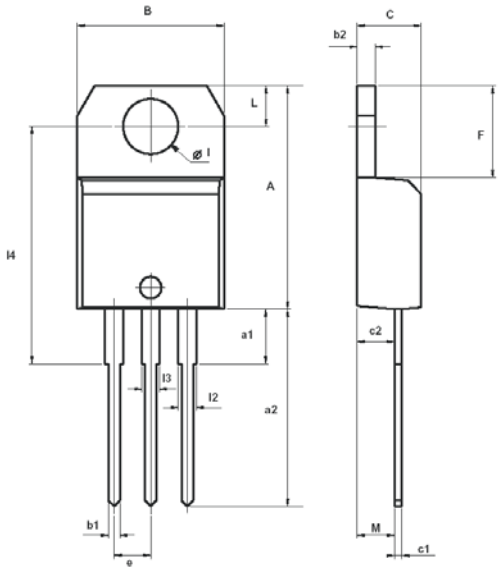

**Fig. 11:** Thermal resistance junction to ambient versus copper surface under tab (Epoxy printed circuit board FR4, copper thickness: 35 µm) .



## HAOPIN MICROELECTRONICS CO.,LTD.

MECHANICAL DATA

Dimensions in mm
Net Mass: 2 g




| REF. | DIMENSIONS | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 15.20 | | 15.90 | 0.598 | | 0.625 |
| a1 | | 3.75 | | | 0.147 | |
| a2 | 13.00 | | 14.00 | 0.511 | | 0.551 |
| B | 10.00 | | 10.40 | 0.393 | | 0.409 |
| b1 | 0.61 | | 0.88 | 0.024 | | 0.034 |
| b2 | 1.23 | | 1.32 | 0.048 | | 0.051 |
| C | 4.40 | | 4.60 | 0.173 | | 0.181 |
| c1 | 0.49 | | 0.70 | 0.019 | | 0.027 |
| c2 | 2.40 | | 2.72 | 0.094 | | 0.107 |
| e | 2.40 | | 2.70 | 0.094 | | 0.106 |
| F | 6.20 | | 6.60 | 0.244 | | 0.259 |
| I | 3.75 | | 3.85 | 0.147 | | 0.151 |
| I4 | 15.80 | 16.40 | 16.80 | 0.622 | 0.646 | 0.661 |
| L | 2.65 | | 2.95 | 0.104 | | 0.116 |
| I2 | 1.14 | | 1.70 | 0.044 | | 0.066 |
| I3 | 1.14 | | 1.70 | 0.044 | | 0.066 |
| M | | 2.60 | | | 0.102 | |