Plastic Medium-Power Complementary Silicon Transistors

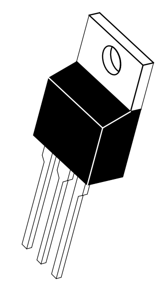
. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector–Emitter Sustaining Voltage — @ 100 mAdc —
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6040, 2N6043
  = 80 Vdc (Min) — 2N6041, 2N6044
  = 100 Vdc (Min) — 2N6042, 2N6045
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 4.0 Adc — 2N6040,41, 2N6043,44
  = 2.0 Vdc (Max) @ I_C = 3.0 Adc — 2N6042, 2N6045
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors

PNP
2N6040
thru
2N6042*
NPN
2N6043
thru
2N6045*

*Motorola Preferred Device

DARLINGTON
8 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60–80–100 VOLTS
75 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS (1)

Rating	Symbol	2N6040 2N6043	2N6041 2N6044	2N6042 2N6045	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	8.0 16			Adc
Base Current	I_B	120			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.60			Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	57	°C/W

(1) Indicates JEDEC Registered Data.

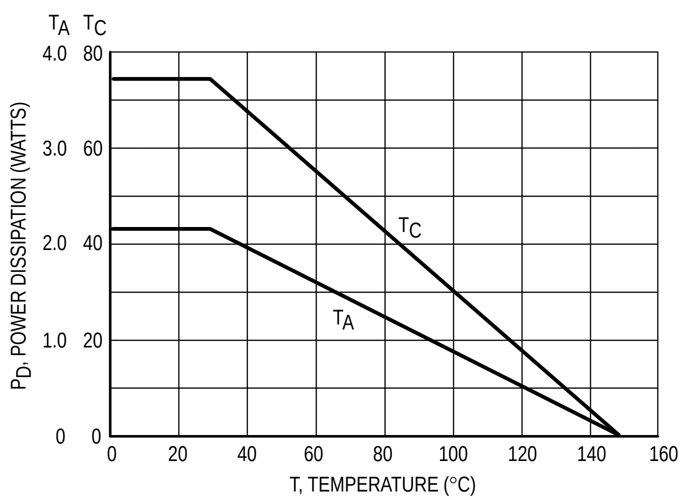


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	2N6040, 2N6043 2N6041, 2N6044 2N6042, 2N6045	$V_{CEO(sus)}$	60 80 100	— — —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0) (V_{CE} = 100 Vdc, I_B = 0)	2N6040, 2N6043 2N6041, 2N6044 2N6042, 2N6045	I_{CEO}	— — —	20 20 20	µA
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6040, 2N6043 2N6041, 2N6044 2N6042, 2N6045 2N6040, 2N6043 2N6041, 2N6044 2N6042, 2N6045	I_{CEX}	— — — — — —	20 20 20 200 200 200	µA
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	2N6040, 2N6043 2N6041, 2N6044 2N6042, 2N6045	I_{CBO}	— — —	20 20 20	µA
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	2N6040, 41, 2N6043, 44 2N6042, 2N6045 All Types	h_{FE}	1000 1000 100	20.000 20,000 —	—
Collector–Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 16 mAdc) (I_C = 3.0 Adc, I_B = 12 mAdc) (I_C = 8.0 Adc, I_B = 80 Adc)	2N6040, 41, 2N6043, 44 2N6042, 2N6045 All Types	$V_{CE(sat)}$	— — —	2.0 2.0 4.0	Vdc
Base–Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 80 mAdc)		$V_{BE(sat)}$	—	4.5	Vdc
Base–Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	—	
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6040/2N6042 2N6043/2N6045	C_{ob}	— —	300 200	pF
Small–Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	300	—	—

* Indicates JEDEC Registered Data.

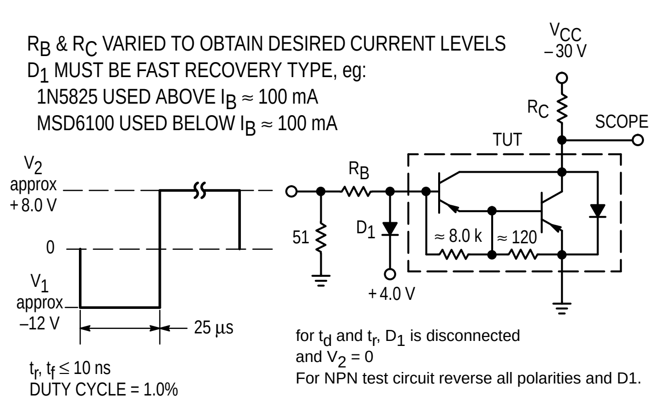


Figure 2. Switching Times Equivalent Circuit

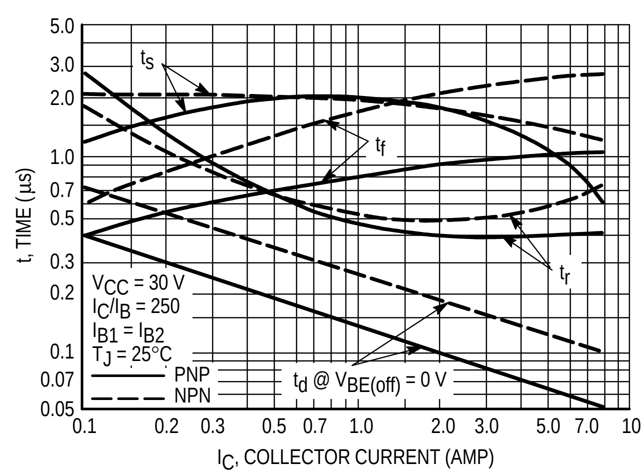


Figure 3. Switching Times

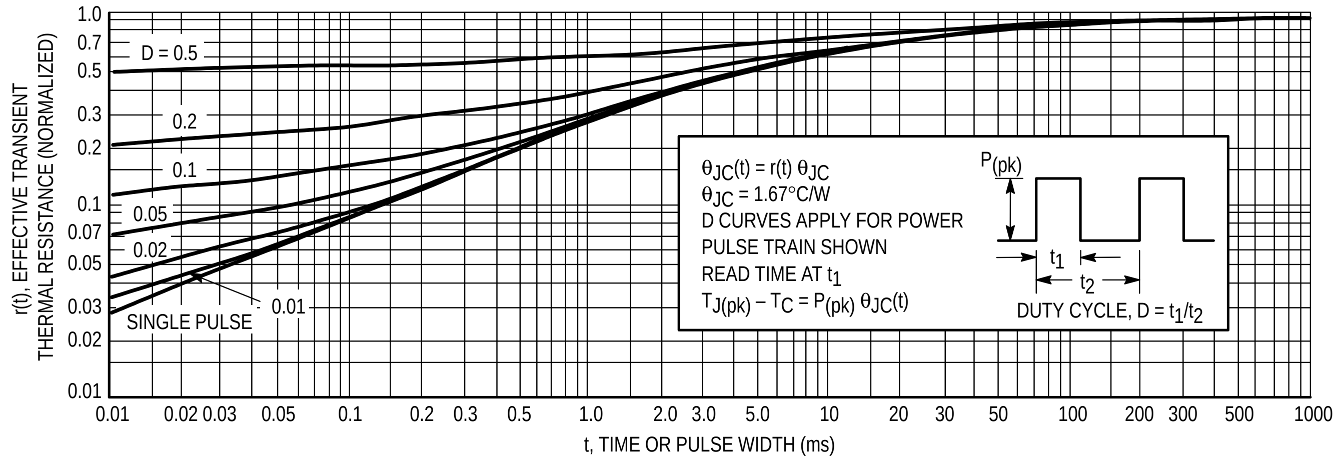


Figure 4. Thermal Response

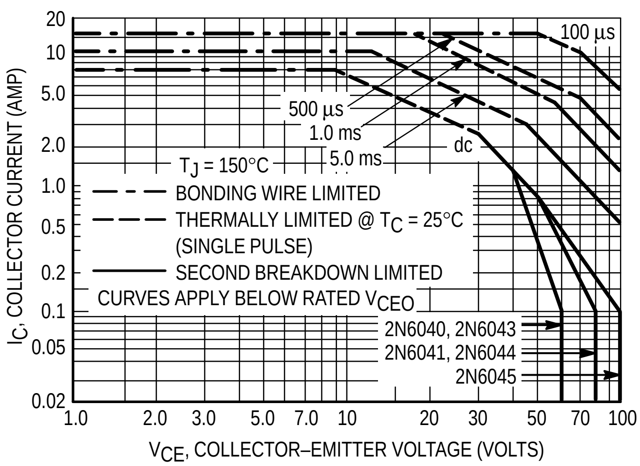


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

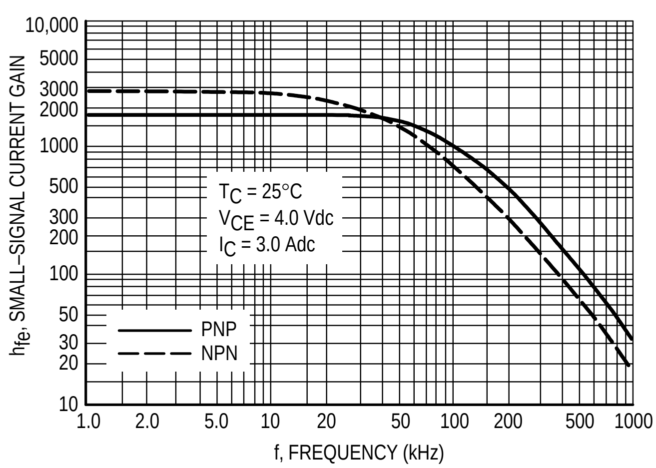


Figure 6. Small–Signal Current Gain

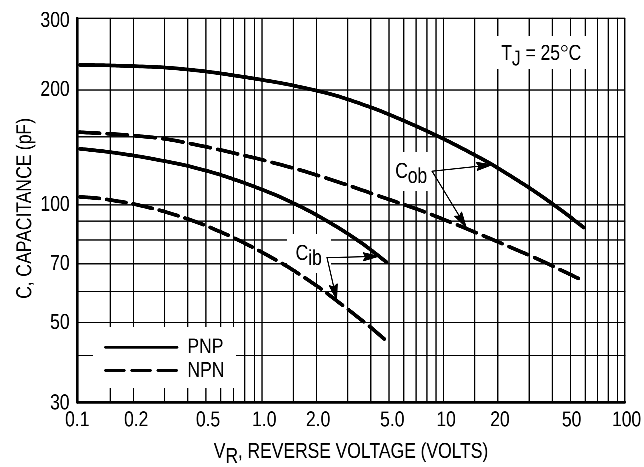


Figure 7. Capacitance

PNP
2N6040, 2N6041, 2N6042

NPN
2N6043, 2N6044, 2N6045

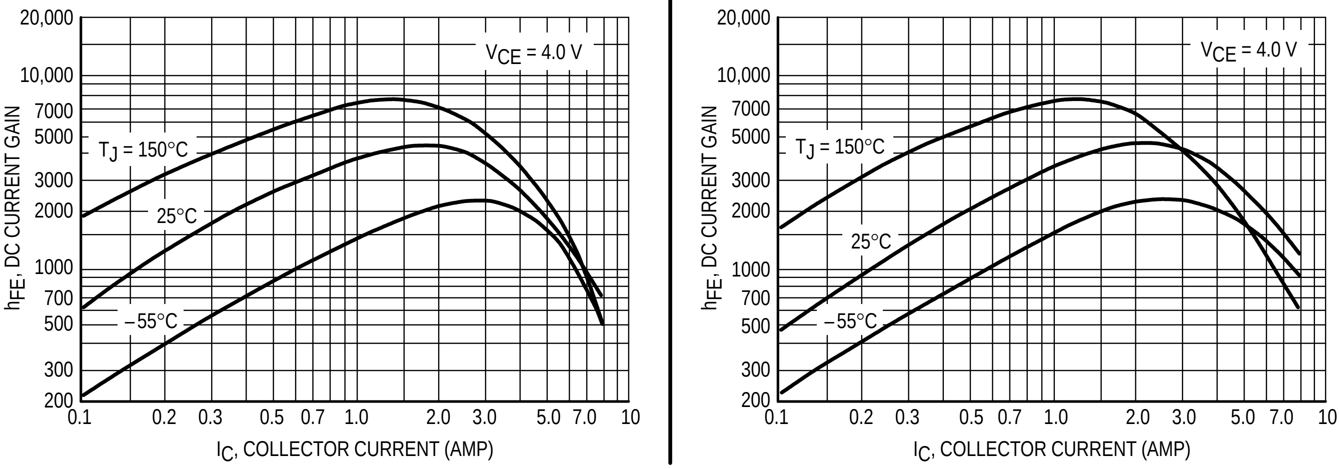


Figure 8. DC Current Gain

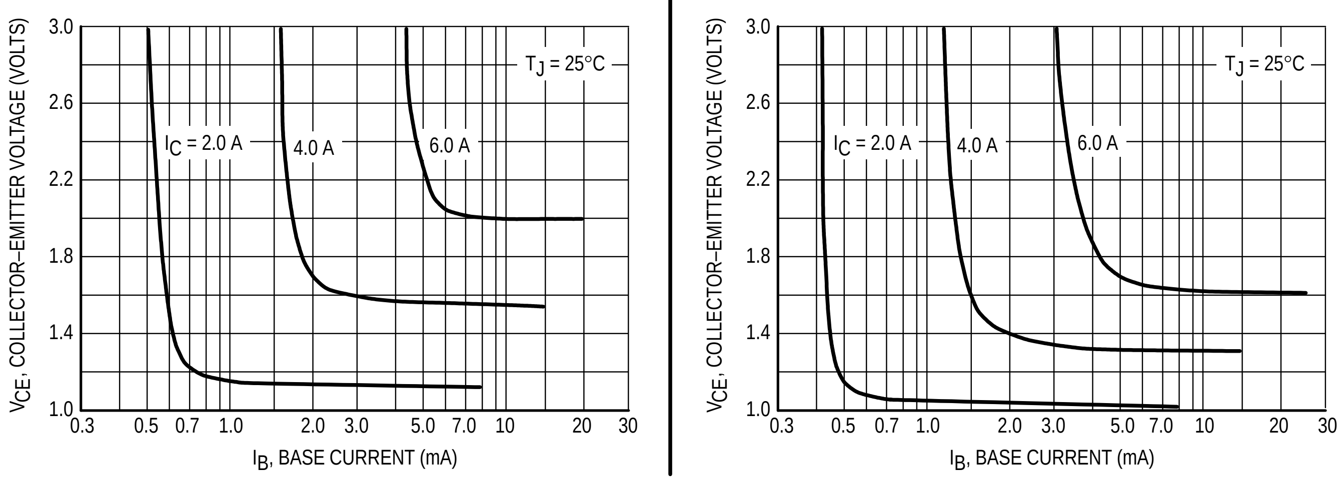


Figure 9. Collector Saturation Region

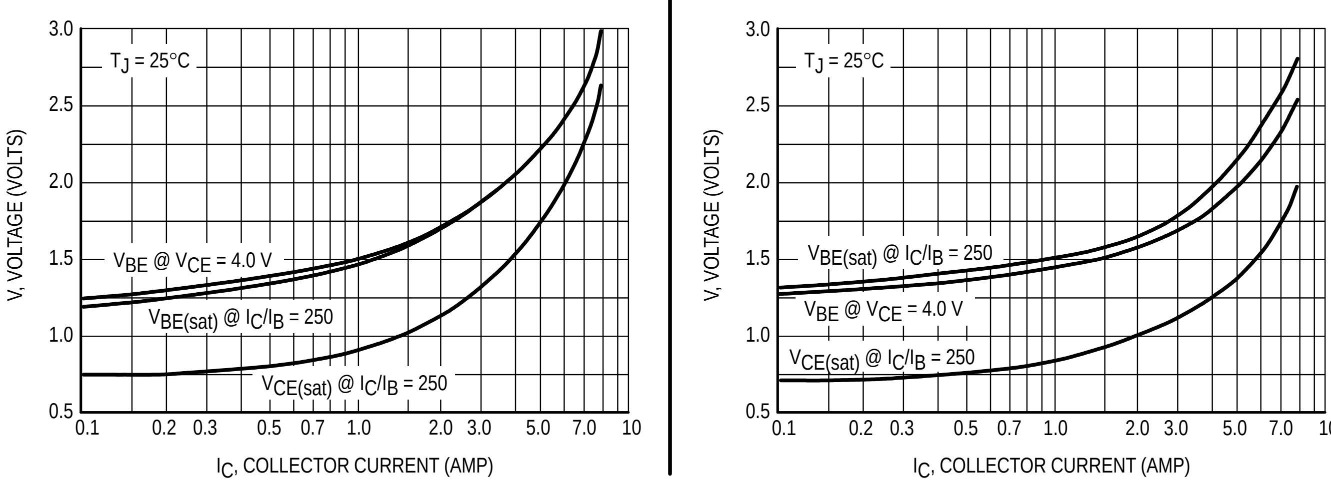
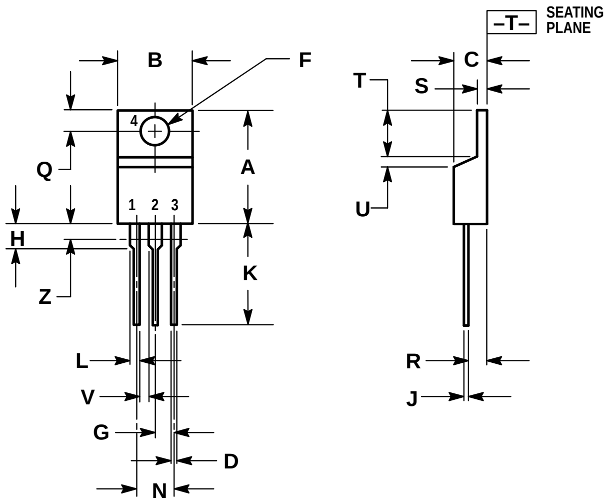


Figure 10. “On” Voltages

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A–06
TO–220AB
ISSUE Y

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