

C504

8-Bit Single-Chip Microcontroller

8bit

Microcontrollers



Never stop thinking.

Edition 2000-05

**Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany**

**© Infineon Technologies AG 2000.
All Rights Reserved.**

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

C504

8-Bit Single-Chip Microcontroller

Microcontrollers



Never stop thinking.

C504

Revision History: **2000-05**

Previous Version: 1996-05

| Page | Subjects (major changes since last revision) |
|-------------|---|
| 35 - 40 | OTP Memory Operation is added. |
| 41 | Table on Version Byte Content is added. |
| 57 - 60 | AC Characteristics of Programming Mode is added. |
| several | V_{CC} is replaced by V_{DD} . |
| several | Specification for SAH-C504 is removed |

Enhanced Hooks Technology™ is a trademark and patent of Metalink Corporation licensed to Infineon Technologies.

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document.

Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com



8-Bit Single-Chip Microcontroller C500 Family

C504

C504

- Fully compatible to standard 8051 microcontroller
- Up to 40 MHz external operating frequency
- 16 Kbyte on-chip program memory
 - C504-2R: ROM version (with optional ROM protection)
 - C504-2E: programmable OTP version
 - C504-L: without on-chip program memory
- 256 byte on-chip RAM
- 256 byte on-chip XRAM
- Four 8-bit ports
 - 2 ports with mixed analog/digital I/O capability
- Three 16-bit timers/counters
 - Timer 2 with up/down counter feature

Further features are listed next page.

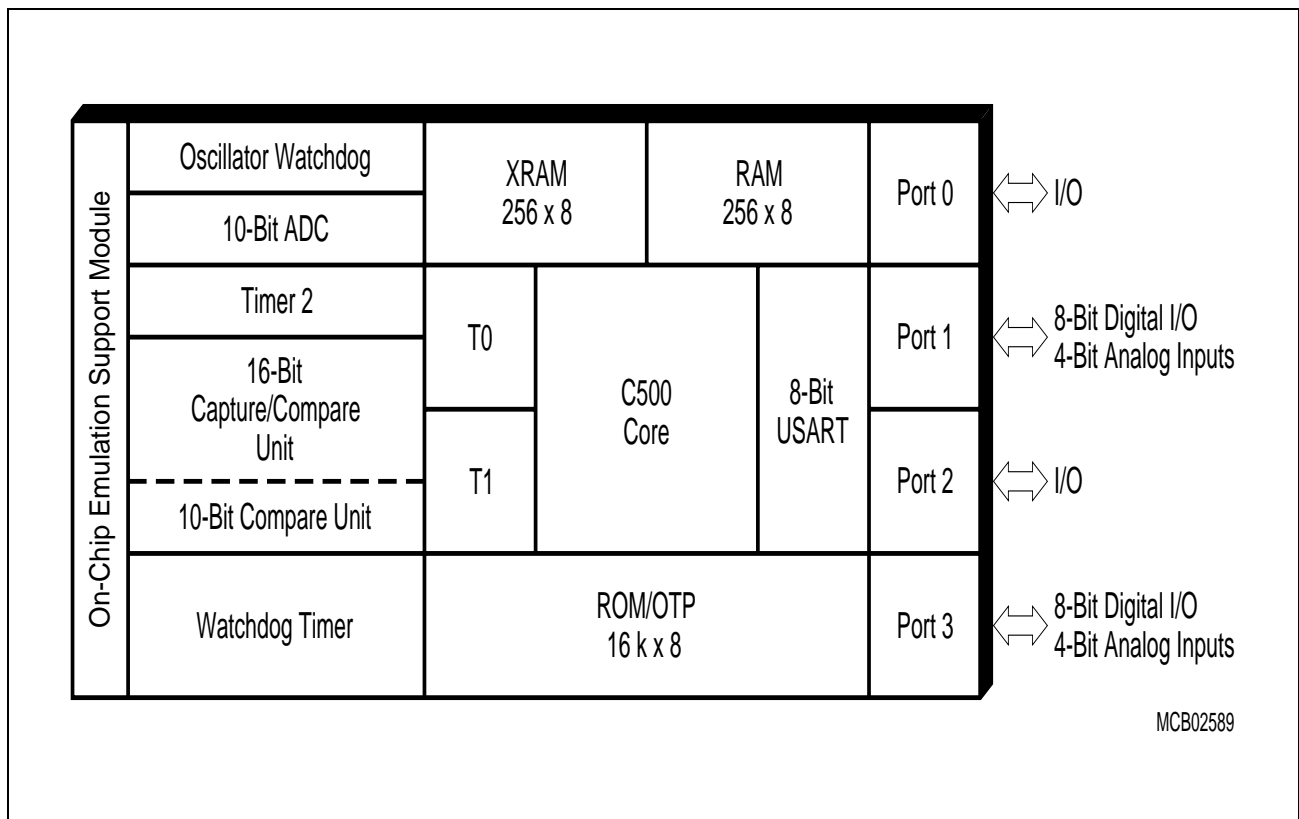


Figure 1 C504 Functional Units

- Capture/compare unit for PWM signal generation and signal capturing
 - 3-channel, 16-bit capture/compare unit
 - 1-channel, 10-bit compare unit
- Full duplex serial interface (USART)
- 10-bit A/D Converter with 8 multiplexed inputs
- Twelve interrupt sources with two priority levels
- On-chip emulation support logic (Enhanced Hooks Technology™)
- Programmable 15-bit Watchdog Timer
- Oscillator Watchdog
- Fast Power On Reset
- Power Saving Modes
 - Idle mode
 - Power-down mode with wake-up capability through $\overline{\text{INT0}}$
- M-QFP-44 package
- Temperature ranges: SAB-C504 T_A : 0 to 70 °C
SAF-C504 T_A : – 40 to 85 °C
SAK-C504 T_A : – 40 to 125 °C
(max. operating frequency: 24 MHz)

Ordering Information

The ordering code for Infineon Technologies microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set
- the specified temperature range
- the package and the type of delivery

For the available ordering codes for the C504, please refer to the “**Product Information Microcontrollers**” which summarizes all available microcontroller variants.

Note: The ordering codes for the Mask-ROM versions are defined for each product after verification of the respective ROM code.

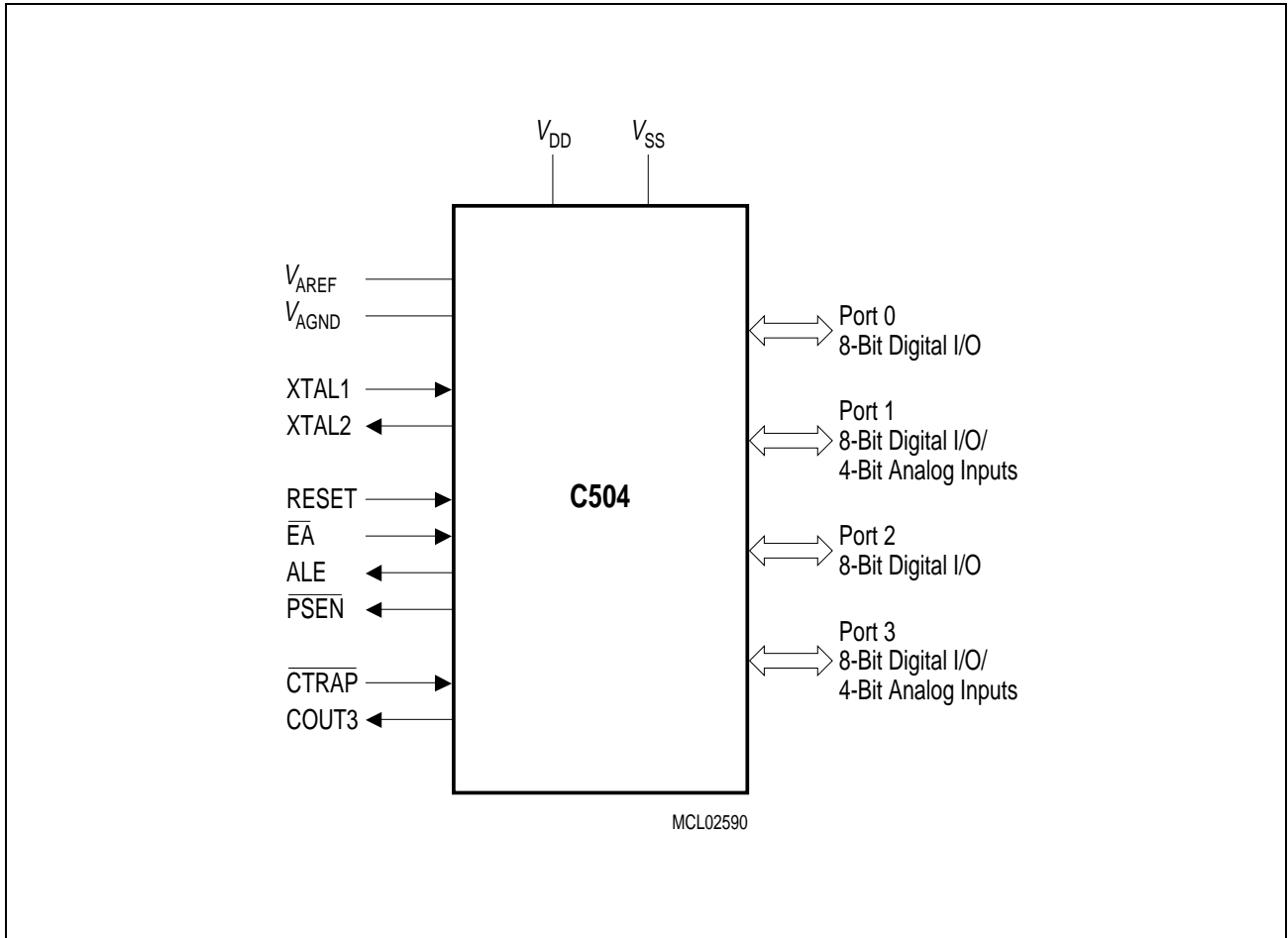


Figure 2 **Logic Symbol**

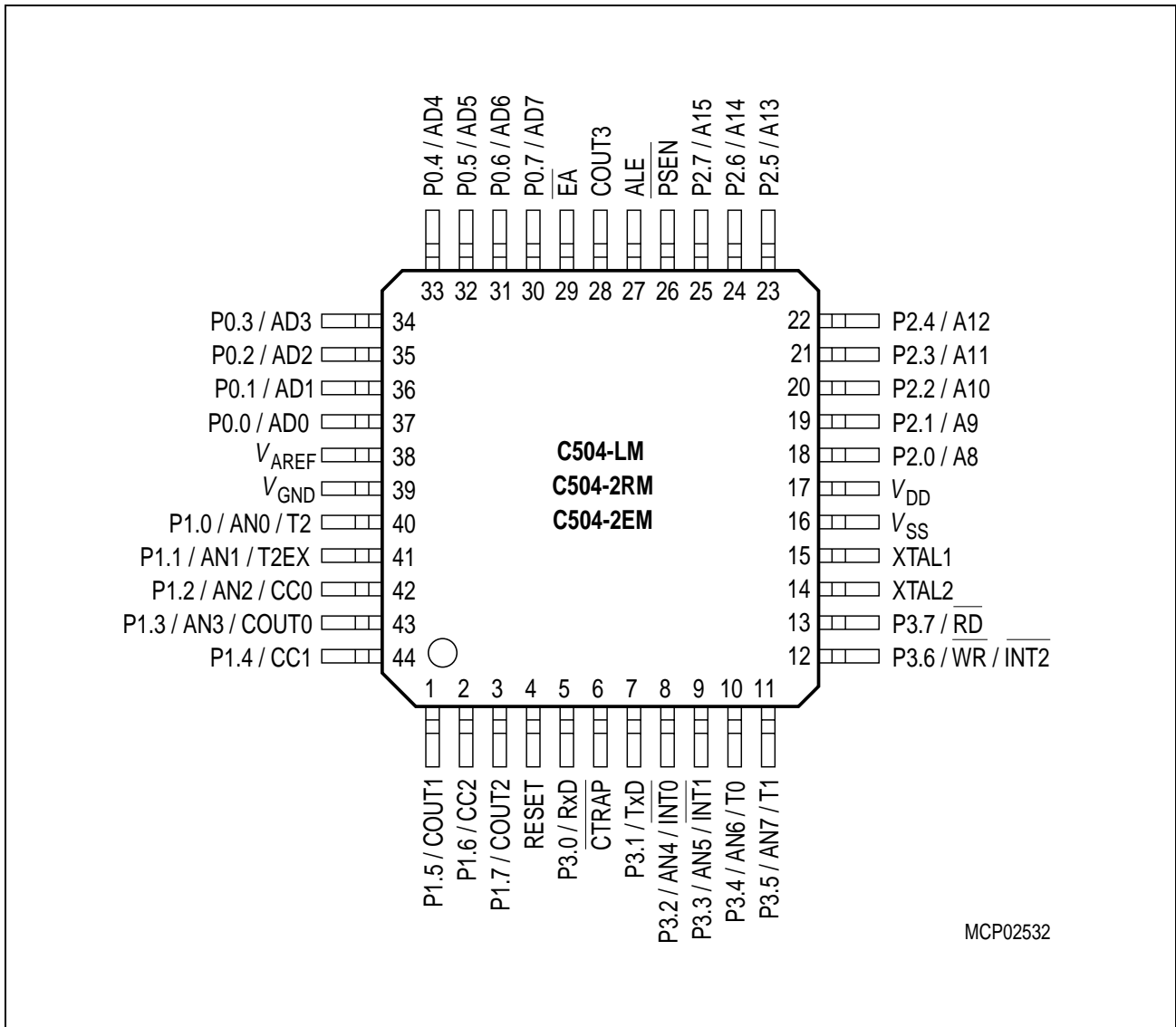


Figure 3 Pin Configuration (top view)

Table 1 Pin Definitions and Functions

| Symbol | Pin Number (P-MQFP-44) | I/O ¹⁾ | Function | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|------------------------|--|--|----|-----------------|---|----|-------------------|--|----|------------------|--|----|--------------------|--|----|------------|---|---|--------------|-------------------------------------|---|------------|---|---|--------------|-------------------------------------|
| P1.0 - P1.7 | 40 - 44, 1 - 3 | I/O | <p>Port 1 is an 8-bit bidirectional port. Port 1 pins can be used for digital input/output. P1.0 - P1.3 can also be used as analog inputs of the A/D converter. As secondary digital functions, Port 1 contains the Timer 2 pins and the Capture/Compare inputs/outputs. Port 1 pins are assigned to be used as analog inputs via the register P1ANA.</p> <p>The functions are assigned to the pins of Port 1 as follows:</p> <table border="0"> <tr> <td>40</td> <td>P1.0 / AN0 / T2</td> <td>Analog input channel 0 / input to Timer 2</td> </tr> <tr> <td>41</td> <td>P1.1 / AN1 / T2EX</td> <td>Analog input channel 1 / capture/reload trigger of Timer 2 up-down count</td> </tr> <tr> <td>42</td> <td>P1.2 / AN2 / CC0</td> <td>Analog input channel 2 / input/output of capture/compare channel 0</td> </tr> <tr> <td>43</td> <td>P1.3 / AN3 / COUT0</td> <td>Analog input channel 3 / output of capture/compare channel 0</td> </tr> <tr> <td>44</td> <td>P1.4 / CC1</td> <td>Input/output of capture/compare channel 1</td> </tr> <tr> <td>1</td> <td>P1.5 / COUT1</td> <td>Output of capture/compare channel 1</td> </tr> <tr> <td>2</td> <td>P1.6 / CC2</td> <td>Input/output of capture/compare channel 2</td> </tr> <tr> <td>3</td> <td>P1.7 / COUT2</td> <td>Output of capture/compare channel 2</td> </tr> </table> | 40 | P1.0 / AN0 / T2 | Analog input channel 0 / input to Timer 2 | 41 | P1.1 / AN1 / T2EX | Analog input channel 1 / capture/reload trigger of Timer 2 up-down count | 42 | P1.2 / AN2 / CC0 | Analog input channel 2 / input/output of capture/compare channel 0 | 43 | P1.3 / AN3 / COUT0 | Analog input channel 3 / output of capture/compare channel 0 | 44 | P1.4 / CC1 | Input/output of capture/compare channel 1 | 1 | P1.5 / COUT1 | Output of capture/compare channel 1 | 2 | P1.6 / CC2 | Input/output of capture/compare channel 2 | 3 | P1.7 / COUT2 | Output of capture/compare channel 2 |
| 40 | P1.0 / AN0 / T2 | Analog input channel 0 / input to Timer 2 | | | | | | | | | | | | | | | | | | | | | | | | | |
| 41 | P1.1 / AN1 / T2EX | Analog input channel 1 / capture/reload trigger of Timer 2 up-down count | | | | | | | | | | | | | | | | | | | | | | | | | |
| 42 | P1.2 / AN2 / CC0 | Analog input channel 2 / input/output of capture/compare channel 0 | | | | | | | | | | | | | | | | | | | | | | | | | |
| 43 | P1.3 / AN3 / COUT0 | Analog input channel 3 / output of capture/compare channel 0 | | | | | | | | | | | | | | | | | | | | | | | | | |
| 44 | P1.4 / CC1 | Input/output of capture/compare channel 1 | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | P1.5 / COUT1 | Output of capture/compare channel 1 | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | P1.6 / CC2 | Input/output of capture/compare channel 2 | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | P1.7 / COUT2 | Output of capture/compare channel 2 | | | | | | | | | | | | | | | | | | | | | | | | | |
| RESET | 4 | I | <p>RESET A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{DD}.</p> | | | | | | | | | | | | | | | | | | | | | | | | |

Table 1 Pin Definitions and Functions (cont'd)

| Symbol | Pin Number (P-MQFP-44) | I/O ¹⁾ | Function | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|--|--|---|---|------------|---|---|------------|--|---|--------------------------------|--|---|--------------------------------|--|----|-----------------|--|----|-----------------|--|----|--|--|----|------------------------|--|
| P3.0 - P3.7 | 5, 7 - 13 | I/O | <p>Port 3 is an 8-bit bidirectional port. P3.0 (RxD) and P3.1 (TxD) operate as defined for the C501. P3.2 to P3.7 contain the external interrupt inputs, timer inputs, and four of the analog inputs of the A/D converter. Port 3 pins are assigned to be used as analog inputs via the bits of SFR P3ANA. P3.6/W\overline{R} can be assigned as a third interrupt input.</p> <p>The functions are assigned to the pins of port 3 as follows:</p> <table border="0"> <tr> <td>5</td> <td>P3.0 / RxD</td> <td>Receiver data input (asynch.) or data input/output (synch.) of serial interface</td> </tr> <tr> <td>7</td> <td>P3.1 / TxD</td> <td>Transmitter data output (asynch.) or clock output (synch.) of serial interface</td> </tr> <tr> <td>8</td> <td>P3.2 / AN4 / $\overline{INT0}$</td> <td>Analog input channel 4 / external interrupt 0 input / Timer 0 gate control input</td> </tr> <tr> <td>9</td> <td>P3.3 / AN5 / $\overline{INT1}$</td> <td>Analog input channel 5 / external interrupt 1 input / Timer 1 gate control input</td> </tr> <tr> <td>10</td> <td>P3.4 / AN6 / T0</td> <td>Analog input channel 6 / Timer 0 counter input</td> </tr> <tr> <td>11</td> <td>P3.5 / AN7 / T1</td> <td>Analog input channel 7 / Timer 1 counter input</td> </tr> <tr> <td>12</td> <td>P3.6 / \overline{WR} / $\overline{INT2}$</td> <td>\overline{WR} control output; latches the data byte from port 0 into the external data memory / external interrupt 2 input</td> </tr> <tr> <td>13</td> <td>P3.7 / \overline{RD}</td> <td>\overline{RD} control output; enables the external data memory</td> </tr> </table> | 5 | P3.0 / RxD | Receiver data input (asynch.) or data input/output (synch.) of serial interface | 7 | P3.1 / TxD | Transmitter data output (asynch.) or clock output (synch.) of serial interface | 8 | P3.2 / AN4 / $\overline{INT0}$ | Analog input channel 4 / external interrupt 0 input / Timer 0 gate control input | 9 | P3.3 / AN5 / $\overline{INT1}$ | Analog input channel 5 / external interrupt 1 input / Timer 1 gate control input | 10 | P3.4 / AN6 / T0 | Analog input channel 6 / Timer 0 counter input | 11 | P3.5 / AN7 / T1 | Analog input channel 7 / Timer 1 counter input | 12 | P3.6 / \overline{WR} / $\overline{INT2}$ | \overline{WR} control output; latches the data byte from port 0 into the external data memory / external interrupt 2 input | 13 | P3.7 / \overline{RD} | \overline{RD} control output; enables the external data memory |
| 5 | P3.0 / RxD | Receiver data input (asynch.) or data input/output (synch.) of serial interface | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | P3.1 / TxD | Transmitter data output (asynch.) or clock output (synch.) of serial interface | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | P3.2 / AN4 / $\overline{INT0}$ | Analog input channel 4 / external interrupt 0 input / Timer 0 gate control input | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | P3.3 / AN5 / $\overline{INT1}$ | Analog input channel 5 / external interrupt 1 input / Timer 1 gate control input | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 | P3.4 / AN6 / T0 | Analog input channel 6 / Timer 0 counter input | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11 | P3.5 / AN7 / T1 | Analog input channel 7 / Timer 1 counter input | | | | | | | | | | | | | | | | | | | | | | | | | |
| 12 | P3.6 / \overline{WR} / $\overline{INT2}$ | \overline{WR} control output; latches the data byte from port 0 into the external data memory / external interrupt 2 input | | | | | | | | | | | | | | | | | | | | | | | | | |
| 13 | P3.7 / \overline{RD} | \overline{RD} control output; enables the external data memory | | | | | | | | | | | | | | | | | | | | | | | | | |

Table 1 Pin Definitions and Functions (cont'd)

| Symbol | Pin Number (P-MQFP-44) | I/O ¹⁾ | Function |
|---------------------------|------------------------|-------------------|---|
| $\overline{\text{CTRAP}}$ | 6 | I | <p>CCU Trap Input</p> <p>With $\text{CTRAP} = \text{low}$, the compare outputs of the CAPCOM unit are switched to the logic level as defined in the COINI register (if they are enabled by the bits in SFR TRCON). $\overline{\text{CTRAP}}$ is an input pin with an internal pullup resistor. For power saving reasons, the signal source which drives the $\overline{\text{CTRAP}}$ input should be at high or floating level during power-down mode.</p> |
| XTAL2 | 14 | – | <p>XTAL2</p> <p>Output of the inverting oscillator amplifier.</p> |
| XTAL1 | 15 | – | <p>XTAL1</p> <p>Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.</p> |
| P2.0 - P2.7 | 18-25 | I/O | <p>Port 2</p> <p>is a bidirectional I/O port with internal pullup resistors. Port 2 pins that have “1”s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, Port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup resistors when issuing “1”s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), Port 2 issues the contents of the P2 special function register.</p> |

Table 1 Pin Definitions and Functions (cont'd)

| Symbol | Pin Number (P-MQFP-44) | I/O ¹⁾ | Function |
|--------------------------|------------------------|-------------------|--|
| $\overline{\text{PSEN}}$ | 26 | O | The Program Store Enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution. |
| ALE | 27 | O | The Address Latch Enable output is used for latching the low-byte of the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access. When instructions are executed from internal ROM ($\overline{\text{EA}} = 1$) the ALE generation can be disabled by clearing bit EALE in SFR SYSCON. |
| COUT3 | 28 | O | 10-Bit compare channel output This pin is used for the output signal of the 10-bit Compare Timer 2 unit. COUT3 can be disabled and set to a high or low state. |
| $\overline{\text{EA}}$ | 29 | I | External Access Enable When held at high level, instructions are fetched from the internal ROM (C504-2R only) when the PC is less than 4000 _H . When held at low level, the C504 fetches all instructions from external program memory. For the C504-L, this pin must be tied low. |
| P0.0 - P0.7 | 37 - 30 | I/O | Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have "1"s written to them float; and in that state, can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application, it uses strong internal pullup resistors when issuing "1" s. Port 0 also outputs the code bytes during program verification in the C504-2R. External pullup resistors are required during program (ROM) verification. |
| V_{AREF} | 38 | – | Reference voltage for the A/D converter. |

Table 1 Pin Definitions and Functions (cont'd)

| Symbol | Pin Number (P-MQFP-44) | I/O ¹⁾ | Function |
|------------|------------------------|-------------------|--|
| V_{AGND} | 39 | – | Reference ground for the A/D converter. |
| V_{SS} | 16 | – | Ground (0 V) |
| V_{DD} | 17 | – | Power Supply (+ 5 V) |

1) I = Input,
O = Output

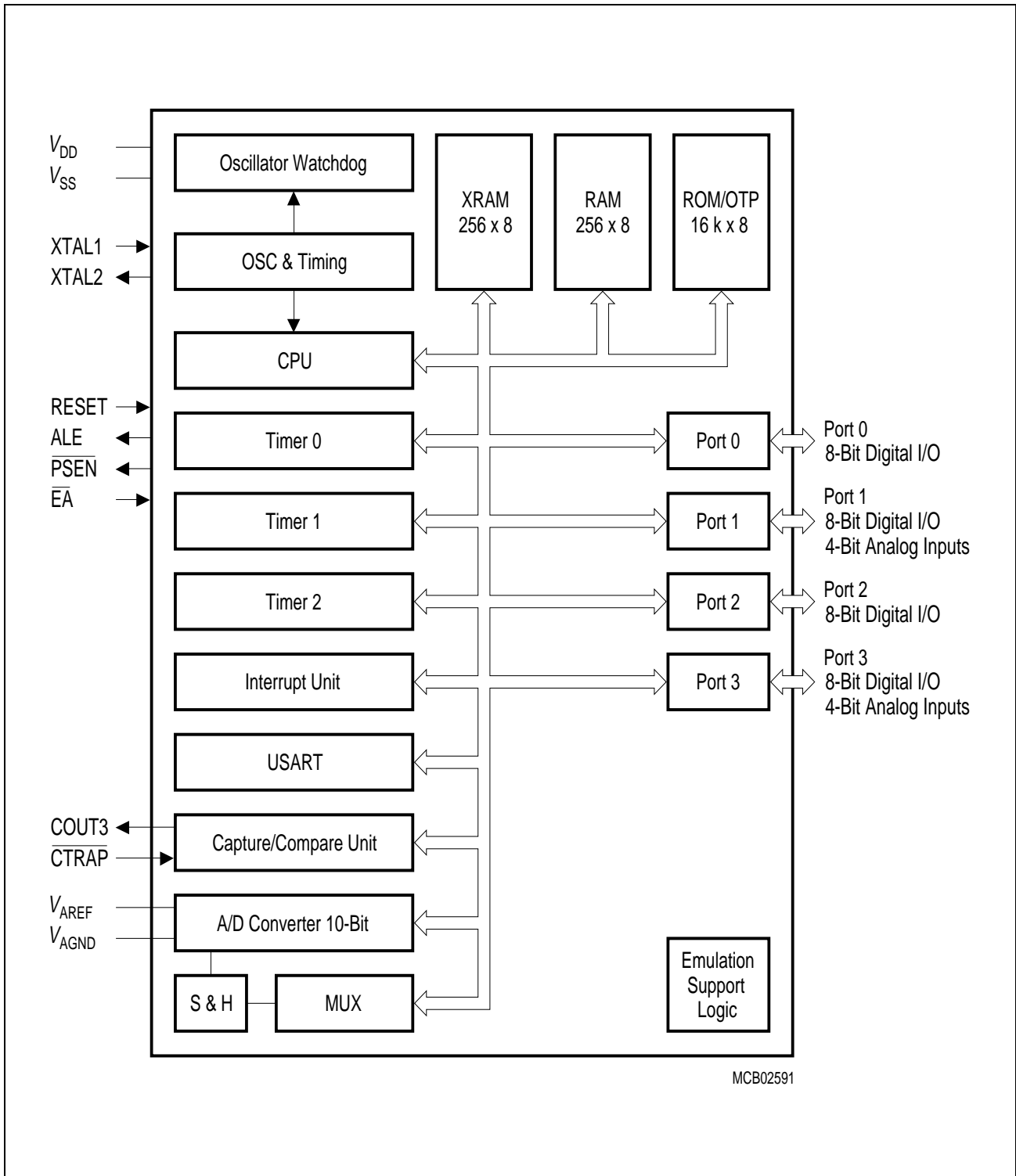


Figure 4 Block Diagram of the C504

CPU

The C504 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions are executed in 1.0 μ s (24 MHz: 500 ns, 40 MHz: 300 ns).

Special Function Register PSW (Address D0_H)

Reset Value: 00_H

| | | | | | | | | | |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----|
| Bit No. | MSB | | | | | | | LSB | |
| | D7 _H | D6 _H | D5 _H | D4 _H | D3 _H | D2 _H | D1 _H | D0 _H | |
| D0 _H | CY | AC | F0 | RS1 | RS0 | OV | F1 | P | PSW |

| Bit | Function | | | | | | | | | | | | | | | |
|------------|--|--|-----|----------|---|---|--|---|---|--|---|---|--|---|---|--|
| CY | Carry Flag Used by arithmetic instructions. | | | | | | | | | | | | | | | |
| AC | Auxiliary Carry Flag Used by instructions which execute BCD operations. | | | | | | | | | | | | | | | |
| F0 | General Purpose Flag 0 | | | | | | | | | | | | | | | |
| RS1 RS0 | Register Bank Select Control bits These bits are used to select one of the four register banks. <table border="1" data-bbox="429 1322 1397 1594"> <thead> <tr> <th>RS1</th> <th>RS0</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Bank 0 selected, data address 00_H-07_H</td> </tr> <tr> <td>0</td> <td>1</td> <td>Bank 1 selected, data address 08_H-0F_H</td> </tr> <tr> <td>1</td> <td>0</td> <td>Bank 2 selected, data address 10_H-17_H</td> </tr> <tr> <td>1</td> <td>1</td> <td>Bank 3 selected, data address 18_H-1F_H</td> </tr> </tbody> </table> | RS1 | RS0 | Function | 0 | 0 | Bank 0 selected, data address 00 _H -07 _H | 0 | 1 | Bank 1 selected, data address 08 _H -0F _H | 1 | 0 | Bank 2 selected, data address 10 _H -17 _H | 1 | 1 | Bank 3 selected, data address 18 _H -1F _H |
| RS1 | RS0 | Function | | | | | | | | | | | | | | |
| 0 | 0 | Bank 0 selected, data address 00 _H -07 _H | | | | | | | | | | | | | | |
| 0 | 1 | Bank 1 selected, data address 08 _H -0F _H | | | | | | | | | | | | | | |
| 1 | 0 | Bank 2 selected, data address 10 _H -17 _H | | | | | | | | | | | | | | |
| 1 | 1 | Bank 3 selected, data address 18 _H -1F _H | | | | | | | | | | | | | | |
| OV | Overflow Flag Used by arithmetic instruction. | | | | | | | | | | | | | | | |
| F1 | General Purpose Flag 1 | | | | | | | | | | | | | | | |
| P | Parity Flag Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator. | | | | | | | | | | | | | | | |

Memory Organization

The C504 CPU manipulates operands in the following four address spaces:

- up to 64 Kbyte of program memory: 16K ROM for C504-2R
16K OTP for C504-2E
- up to 64 Kbyte of external data memory
- 256 bytes of internal data memory
- 256 bytes of internal XRAM data memory
- a 128 byte special function register area

Figure 5 illustrates the memory address spaces of the C504.

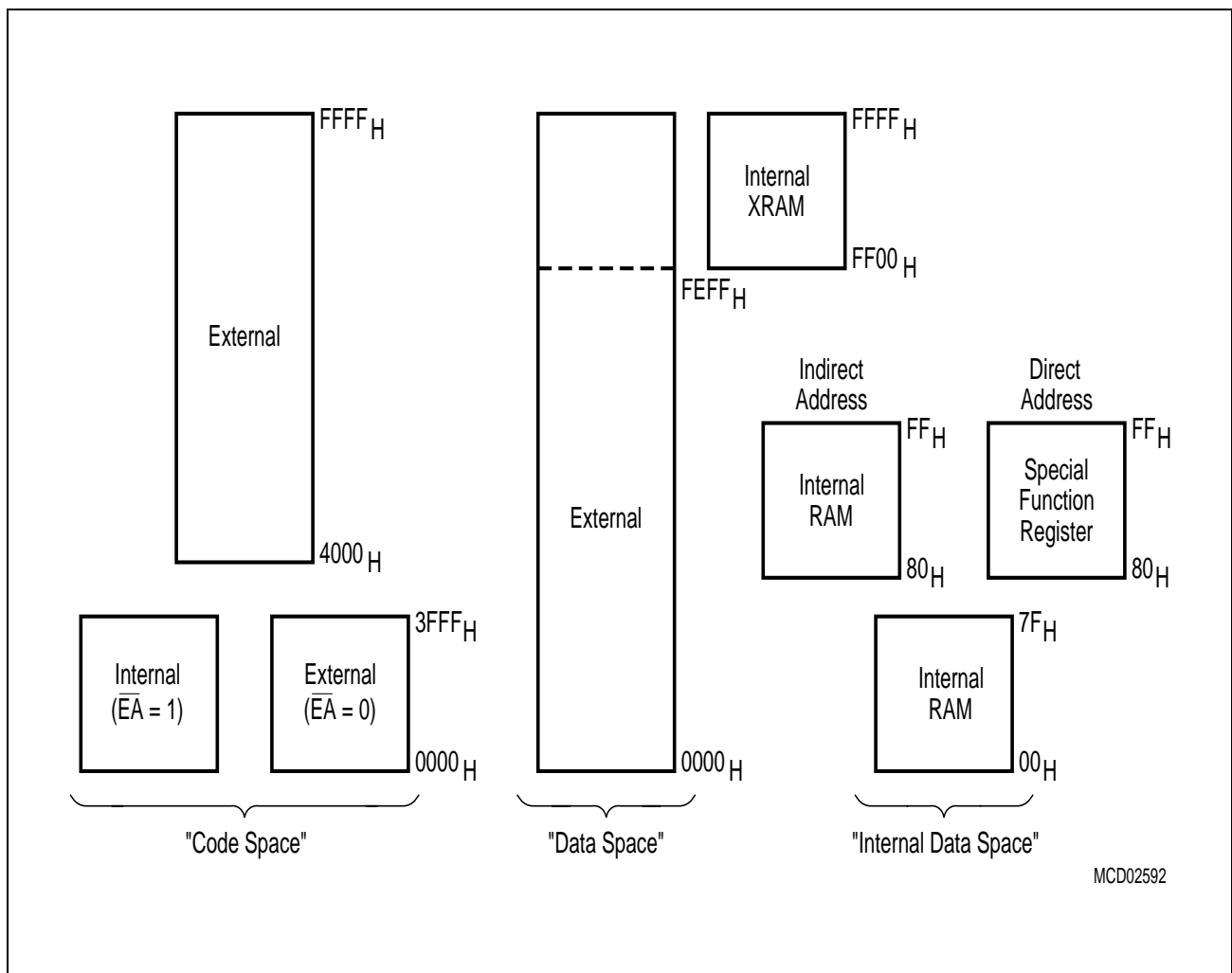


Figure 5 C504 Memory Map

Reset and System Clock Operation

The reset input is an active high input. An internal Schmitt trigger is used at the input for noise rejection. Since the reset is synchronized internally, the RESET pin must be held high for at least two machine cycles (24 oscillator periods) while the oscillator is running.

During reset, pins ALE and $\overline{\text{PSEN}}$ are configured as inputs and should not be stimulated externally. (An external stimulation at these lines during reset activates several test modes which are reserved for test purposes. This, in turn, may cause unpredictable output operations at several port pins).

At the reset pin, a pulldown resistor is internally connected to V_{SS} to allow a power-up reset with an external capacitor only. An automatic reset can be obtained when V_{DD} is applied by connecting the reset pin to V_{DD} via a capacitor. After V_{DD} has been turned on, the capacitor must hold the voltage level at the reset pin for a specific time to effect a complete reset.

The time required for a reset operation is the oscillator start-up time and the time for 2 machine cycles, which must be at least 10 - 20 ms, under normal conditions. This requirement is typically met using a capacitor of 4.7 to 10 μF . The same considerations apply if the reset signal is generated externally (**Figure 6b**). In each case, it must be assured that the oscillator has started up properly and that at least two machine cycles have passed before the reset signal goes inactive.

Figure 6 shows the possible reset circuitries.

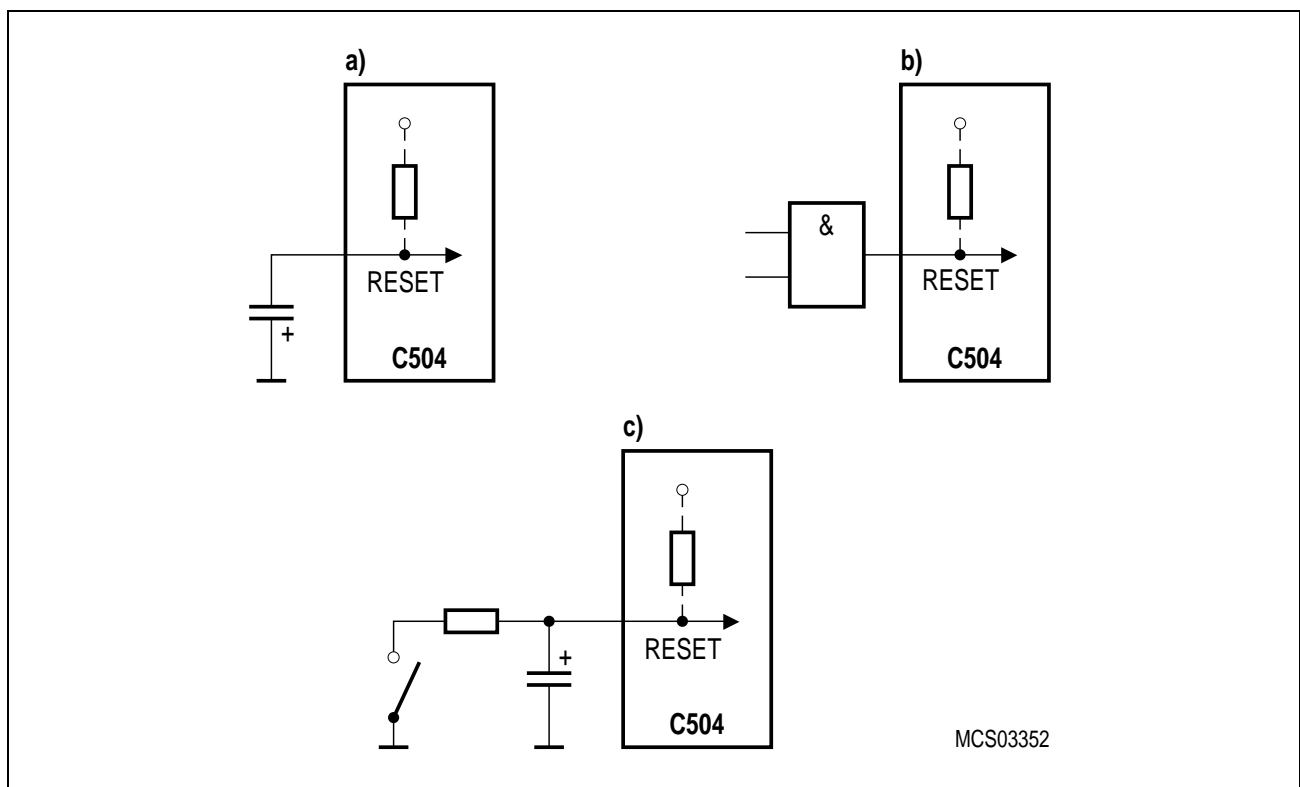


Figure 6 Reset Circuitries

Figure 7 shows the recommended oscillator circuit for the C504, while **Figure 8** shows the circuit for using an external clock source.

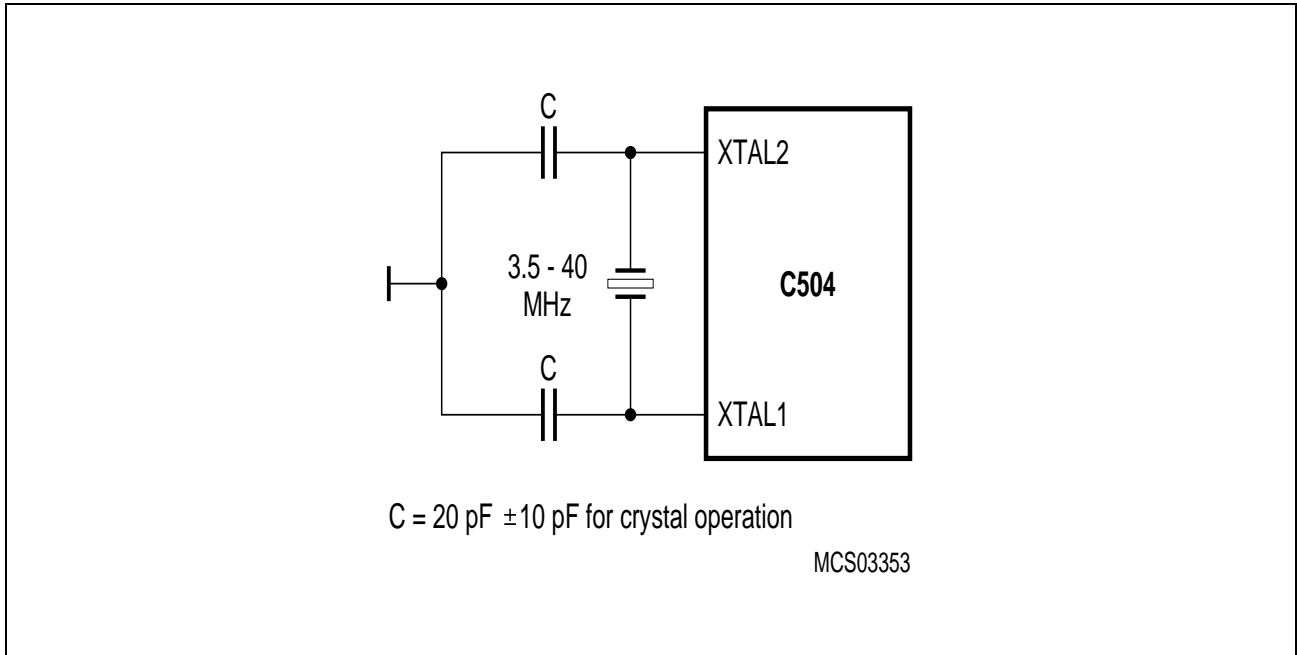


Figure 7 Recommended Oscillator Circuit

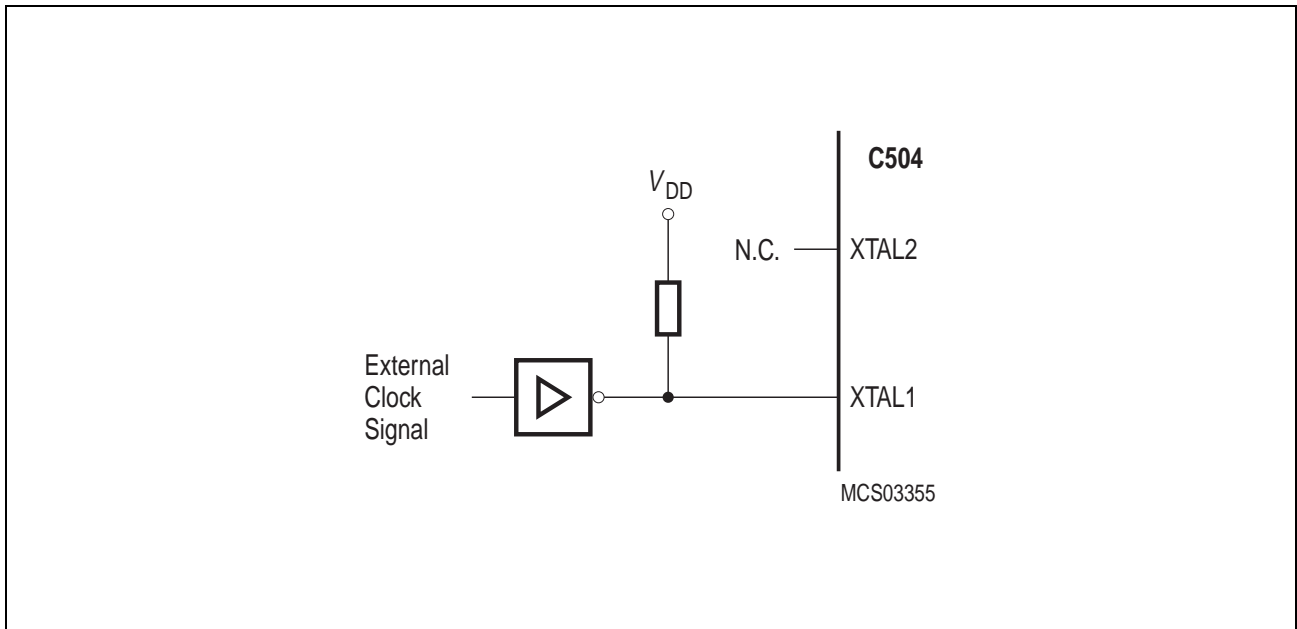


Figure 8 External Clock Source

Enhanced Hooks Emulation Concept

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too.

Each production chip has built-in logic for the support of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology™, which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.

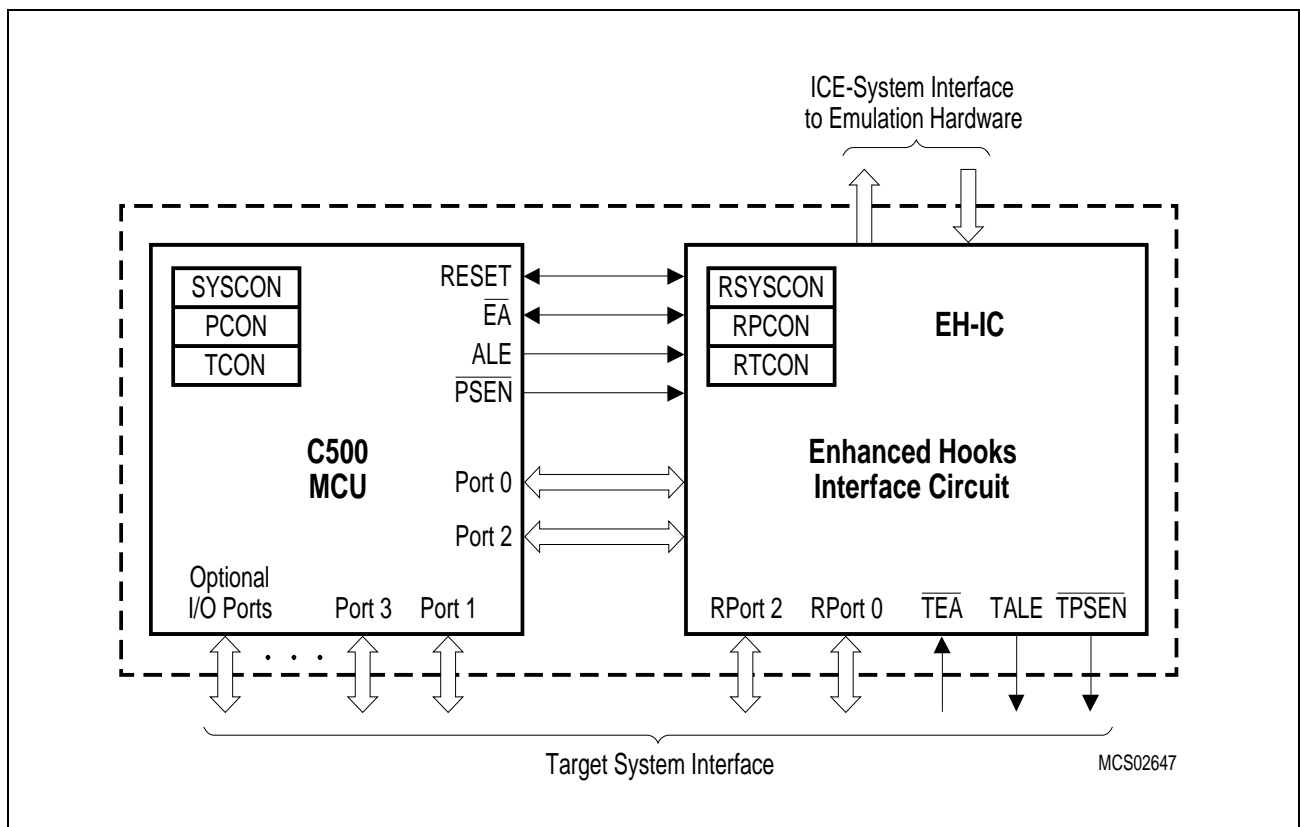


Figure 9 Basic C500 MCU Enhanced Hooks Concept Configuration

Port 0, Port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the program execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 63 special function registers (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. All SFRs with addresses where address bits 0-2 are 0 (e.g. 80_H, 88_H, 90_H, 98_H, ..., F0_H, F8_H) are bit-addressable.

The SFRs of the C504 are listed in **Table 2** and **Table 3**. In **Table 2**, they are organized in groups which refer to the functional blocks of the C504. **Table 3** illustrates the contents of the SFRs in numeric order of their addresses.

Table 2 Special Function Registers - Functional Blocks

| Block | Symbol | Name | Addr. | Contents after Reset |
|---------------------|---------------------|--|--|-------------------------------------|
| CPU | ACC | Accumulator | E0_H ¹⁾ | 00 _H |
| | B | B-Register | F0_H ¹⁾ | 00 _H |
| | DPH | Data Pointer, High Byte | 83 _H | 00 _H |
| | DPL | Data Pointer, Low Byte | 82 _H | 00 _H |
| | PSW | Program Status Word Register | D0_H ¹⁾ | 00 _H |
| | SP | Stack Pointer | 81 _H | 07 _H |
| | SYSCON | System Control Register | B1 _H | XX10XXX0 _B ³⁾ |
| Interrupt System | IEN0 | Interrupt Enable Register 0 | A8_H ¹⁾ | 0X000000 _B ³⁾ |
| | IEN1 | Interrupt Enable Register 1 | A9 _H | XX000000 _B ³⁾ |
| | CCIE ²⁾ | Capture/Compare Interrupt Enable Reg. | D6 _H | 00 _H |
| | IP0 | Interrupt Priority Register 0 | B8_H ¹⁾ | XX000000 _B ³⁾ |
| | IP1 | Interrupt Priority Register 1 | B9 _H | XX000000 _B ³⁾ |
| | ITCON | Interrupt Trigger Condition Register | 9A _H | 00101010 _B |
| Ports | P0 | Port 0 | 80_H ¹⁾ | FF _H |
| | P1 | Port 1 | 90_H ¹⁾ | FF _H |
| | P1ANA ²⁾ | Port 1 Analog Input Selection Register | 90_H ^{1) 4)} | XXXX1111 _B ³⁾ |
| | P2 | Port 2 | A0_H ¹⁾ | FF _H |
| | P3 | Port 3 | B0_H ¹⁾ | FF _H |
| | P3ANA ²⁾ | Port 3 Analog Input Selection Register | B0_H ^{1) 4)} | XX1111XX _B ³⁾ |
| A/D-Converter | ADCON0 | A/D Converter Control Register 0 | D8_H ¹⁾ | XX000000 _B ³⁾ |
| | ADCON1 | A/D Converter Control Register 1 | DC _H | 01XXX000 _B ³⁾ |
| | ADDATH | A/D Converter Data Register High Byte | D9 _H | 00 _H |
| | ADDATL | A/D Converter Data Register Low Byte | DA _H | 00XXXXXX _B ³⁾ |
| | P1ANA ²⁾ | Port 1 Analog Input Selection Register | 90_H ^{1) 4)} | XXXX1111 _B ³⁾ |
| | P3ANA ²⁾ | Port 3 Analog Input Selection Register | B0_H ^{1) 4)} | XX1111XX _B ³⁾ |
| Serial Channels | PCON ²⁾ | Power Control Register | 87 _H | 000X0000 _B |
| | SBUF | Serial Channel Buffer Register | 99 _H | XX _H ³⁾ |
| | SCON | Serial Channel Control Register | 98_H ¹⁾ | 00 _H |
| Timer 0/ Timer 1 | TCON | Timer 0/1 Control Register | 88_H ¹⁾ | 00 _H |
| | TH0 | Timer 0, High Byte | 8C _H | 00 _H |
| | TH1 | Timer 1, High Byte | 8D _H | 00 _H |
| | TL0 | Timer 0, Low Byte | 8A _H | 00 _H |
| | TL1 | Timer 1, Low Byte | 8B _H | 00 _H |
| | TMOD | Timer Mode Register | 89 _H | 00 _H |

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) X means that the value is undefined and the location is reserved

4) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 2 Special Function Registers - Functional Blocks (cont'd)

| Block | Symbol | Name | Addr. | Contents after Reset |
|--------------------|------------------------|---|--|--------------------------------------|
| Timer 2 | T2CON | Timer 2 Control Register | C8_H ¹⁾ | 00 _H |
| | T2MOD | Timer 2 Mode Register | C9 _H | XXXXXXXX0 _B ³⁾ |
| | RC2H | Timer 2 Reload Capture Register, High Byte | CB _H | 00 _H |
| | RC2L | Timer 2 Reload Capture Register, Low Byte | CA _H | 00 _H |
| | TH2 | Timer 2 High Byte | CD _H | 00 _H |
| | TL2 | Timer 2 Low Byte | CC _H | 00 _H |
| | Capture / Compare Unit | CT1CON | Compare timer 1 control register | E1 _H |
| CCPL | | Compare timer 1 period register, low byte | DE _H | 00 _H |
| CCPH | | Compare timer 1 period register, high byte | DF _H | 00 _H |
| CT1OFL | | Compare timer 1 offset register, low byte | E6 _H | 00 _H |
| CT1OFH | | Compare timer 1 offset register, high byte | E7 _H | 00 _H |
| CMSEL0 | | Capture/compare mode select register 0 | E3 _H | 00 _H |
| CMSEL1 | | Capture/compare mode select register 1 | E4 _H | 00 _H |
| COINI | | Compare output initialization register | E2 _H | FF _H |
| TRCON | | Trap enable control register | CF _H | 00 _H |
| CCL0 | | Capture/compare register 0, low byte | C2 _H | 00 _H |
| CCH0 | | Capture/compare register 0, high byte | C3 _H | 00 _H |
| CCL1 | | Capture/compare register 1, low byte | C4 _H | 00 _H |
| CCH1 | | Capture/compare register 1, high byte | C5 _H | 00 _H |
| CCL2 | | Capture/compare register 2, low byte | C6 _H | 00 _H |
| CCH2 | | Capture/compare register 2, high byte | C7 _H | 00 _H |
| CCIR | | Capture/compare interrupt request flag reg. | E5 _H | 00 _H |
| CCIE ²⁾ | | Capture/compare interrupt enable register | D6 _H | 00 _H |
| CT2CON | | Compare timer 2 control register | C1 _H | 00010000 _B |
| CP2L | | Compare timer 2 period register, low byte | D2 _H | 00 _H |
| CP2H | | Compare timer 2 period register, high byte | D3 _H | XXXXXX00 _B ³⁾ |
| CMP2L | | Compare timer 2 compare register, low byte | D4 _H | 00 _H |
| CMP2H | | Compare timer 2 compare register, high byte | D5 _H | XXXXXX00 _B ³⁾ |
| BCON | | Block commutation control register | D7 _H | 00 _H |
| Watchdog Timer | WDCON | Watchdog Timer Control Register | C0_H ¹⁾ | XXXX0000 _B ³⁾ |
| | WDTREL | Watchdog Timer Reload Register | 86 _H | 00 _H |
| Power Saving Mode | PCON ²⁾ | Power Control Register | 87 _H | 000X0000 _B ³⁾ |
| | PCON1 | Power Control Register 1 | 88_H ^{1) 4)} | 0XXXXXXXX _B ³⁾ |

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) X means that the value is undefined and the location is reserved

4) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 3 Contents of the SFRs, SFRs in Numeric Order of their Addresses

| Addr | Register | Content after Reset ¹⁾ | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------------------------|----------|-----------------------------------|-------------|--------------|-------|-------|-------|--------------|-------|-------|
| 80 _H ²⁾ | P0 | FF _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| 81 _H | SP | 07 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| 82 _H | DPL | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| 83 _H | DPH | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| 86 _H | WDTREL | 00 _H | WDT PSEL | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| 87 _H | PCON | 000X- 0000 _B | SMOD | PDS | IDLS | – | GF1 | GF0 | PDE | IDLE |
| 88 _H ²⁾ | TCON | 00 _H | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 |
| 88 _H ¹⁾³⁾ | PCON1 | 0XXX- XXXX _B | EWPD | – | – | – | – | – | – | – |
| 89 _H | TMOD | 00 _H | GATE | C/ \bar{T} | M1 | M0 | GATE | C/ \bar{T} | M1 | M0 |
| 8A _H | TL0 | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| 8B _H | TL1 | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| 8C _H | TH0 | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| 8D _H | TH1 | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| 90 _H ²⁾ | P1 | FF _H | .7 | .6 | .5 | .4 | .3 | .2 | T2EX | T2 |
| 90 _H ²⁾³⁾ | P1ANA | XXXX- 1111 _B | – | – | – | – | EAN3 | EAN2 | EAN1 | EAN0 |
| 98 _H ²⁾ | SCON | 00 _H | SM0 | SM1 | SM2 | REN | TB8 | RB8 | TI | RI |
| 99 _H | SBUF | XX _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| 9A _H | ITCON | 0010- 1010 _B | IT2 | IE2 | I2ETF | I2ETR | I1ETF | I1ETR | I0ETF | I0ETR |
| A0 _H ²⁾ | P2 | FF _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| A8 _H ²⁾ | IEN0 | 0X00- 0000 _B | EA | – | ET2 | ES | ET1 | EX1 | ET0 | EX0 |
| A9 _H | IEN1 | XX00- 0000 _B | – | – | ECT1 | ECCM | ECT2 | ECM | EX2 | EADC |

1) X means that the value is undefined and the location is reserved

2) Bit-addressable special function registers

3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 3 Contents of the SFRs, SFRs in Numeric Order of their Addresses (cont'd)

| Addr | Register | Content after Reset ¹⁾ | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------------------------|----------|-----------------------------------|-------|-------|-------|---------|-------|-------|------------------|--------|
| B0 _H ²⁾ | P3 | FF _H | RD | WR | T1 | T0 | INT1 | INT0 | TxD | RxD |
| B0 _H ²⁾³⁾ | P3ANA | XX11-11XX _B | – | – | EAN7 | EAN6 | EAN5 | EAN4 | – | – |
| B1 _H | SYSCON | XX10-XXX0 _B | – | – | EALE | RMAP | – | – | – | XMAP |
| B8 _H ²⁾ | IP0 | XX00-0000 _B | – | – | PT2 | PS | PT1 | PX1 | PT0 | PX0 |
| B9 _H | IP1 | XX00-0000 _B | – | – | PCT1 | PCCM | PCT2 | PCEM | PX2 | PADC |
| C0 _H ²⁾ | WDCON | XXXX-0000 _B | – | – | – | – | OWDS | WDTS | WDT | SWDT |
| C1 _H | CT2CON | 0001-0000 _B | CT2P | ECT2O | STE2 | CT2 RES | CT2R | CLK2 | CLK1 | CLK0 |
| C2 _H | CCL0 | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| C3 _H | CCH0 | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| C4 _H | CCL1 | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| C5 _H | CCH1 | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| C6 _H | CCL2 | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| C7 _H | CCH2 | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| C8 _H ²⁾ | T2CON | 00 _H | TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | C/T ₂ | CP/RL2 |
| C9 _H | T2MOD | XXXX-XXX0 _B | – | – | – | – | – | – | – | DCEN |
| CA _H | RC2L | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| CB _H | RC2H | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| CC _H | TL2 | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| CD _H | TH2 | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| CF _H | TRCON | 00 _H | TRPEN | TRF | TREN5 | TREN4 | TREN3 | TREN2 | TREN1 | TREN0 |

1) X means that the value is undefined and the location is reserved

2) Bit-addressable special function registers

3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 3 Contents of the SFRs, SFRs in Numeric Order of their Addresses (cont'd)

| Addr | Register | Content after Reset ¹⁾ | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------------------|----------|-----------------------------------|--------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| D0 _H ²⁾ | PSW | 00 _H | CY | AC | F0 | RS1 | RS0 | OV | F1 | P |
| D2 _H | CP2L | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| D3 _H | CP2H | XXXX. XX00 _B | – | – | – | – | – | – | .1 | .0 |
| D4 _H | CMP2L | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| D5 _H | CMP2H | XXXX. XX00 _B | – | – | – | – | – | – | .1 | .0 |
| D6 _H | CCIE | 00 _H | ECTP | ECTC | CC2 FEN | CC2 REN | CC1 FEN | CC1 REN | CC0 FEN | CC0 REN |
| D7 _H | BCON | 00 _H | BCMP BCEM | PWM1 | PWM0 | EBCE | BCERR | BCEN | BCM1 | BCM0 |
| D8 _H ²⁾ | ADCON0 | XX00- 0000 _B | – | – | IADC | BSY | ADM | MX2 | MX1 | MX0 |
| D9 _H | ADDATH | 00 _H | .9 | .8 | .7 | .6 | .5 | .4 | .3 | .2 |
| DA _H | ADDATL | 00XX- XXXX _B | .1 | .0 | – | – | – | – | – | – |
| DC _H | ADCON1 | 01XX- X000 _B | ADCL1 | ADCL0 | – | – | – | MX2 | MX1 | MX0 |
| DE _H | CCPL | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| DF _H | CCPH | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| E0 _H ²⁾ | ACC | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| E1 _H | CT1CON | 0001- 0000 _B | CTM | ETRP | STE1 | CT1 RES | CT1R | CLK2 | CLK1 | CLK0 |
| E2 _H | COINI | FF _H | COUT 3I | COUTX I | COUT 2I | CC2I | COUT 1I | CC1I | COUT 0I | CC0I |
| E3 _H | CMSEL0 | 00 _H | CMSEL 13 | CMSEL 12 | CMSEL 11 | CMSEL 10 | CMSEL 03 | CMSEL 02 | CMSEL 01 | CMSEL 00 |
| E4 _H | CMSEL1 | 00 _H | 0 | 0 | 0 | 0 | CMSEL 23 | CMSEL 22 | CMSEL 21 | CMSEL 20 |
| E5 _H | CCIR | 00 _H | CT1FP | CT1FC | CC2F | CC2R | CC1F | CC1R | CC0F | CC0R |
| E6 _H | CT1OFL | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| E7 _H | CT1OFH | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |
| F0 _H ²⁾ | B | 00 _H | .7 | .6 | .5 | .4 | .3 | .2 | .1 | .0 |

1) X means that the value is undefined and the location is reserved

2) Bit-addressable special function registers

Timer/Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **Table 4**.

Table 4 Timer/Counter 0 and 1 Operating Modes

| Mode | Description | TMOD | | | | Input Clock | |
|------|--|------|-----|----|----|------------------------|------------------------|
| | | Gate | C/T | M1 | M0 | internal | external (max.) |
| 0 | 8-bit timer/counter with a divide-by-32 prescaler | X | X | 0 | 0 | $f_{osc}/12 \times 32$ | $f_{osc}/24 \times 32$ |
| 1 | 16-bit timer/counter | X | X | 1 | 1 | $f_{osc}/12$ | $f_{osc}/24$ |
| 2 | 8-bit timer/counter with 8-bit auto-reload | X | X | 0 | 0 | $f_{osc}/12$ | $f_{osc}/24$ |
| 3 | Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops | X | X | 1 | 1 | $f_{osc}/12$ | $f_{osc}/24$ |

In the “timer” function ($C/\bar{T} = '0'$), the register is incremented every machine cycle. Therefore the count rate is $f_{osc}/12$.

In the “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{osc}/24$. External inputs INT0 and INT1 (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 10** illustrates the input clock logic.

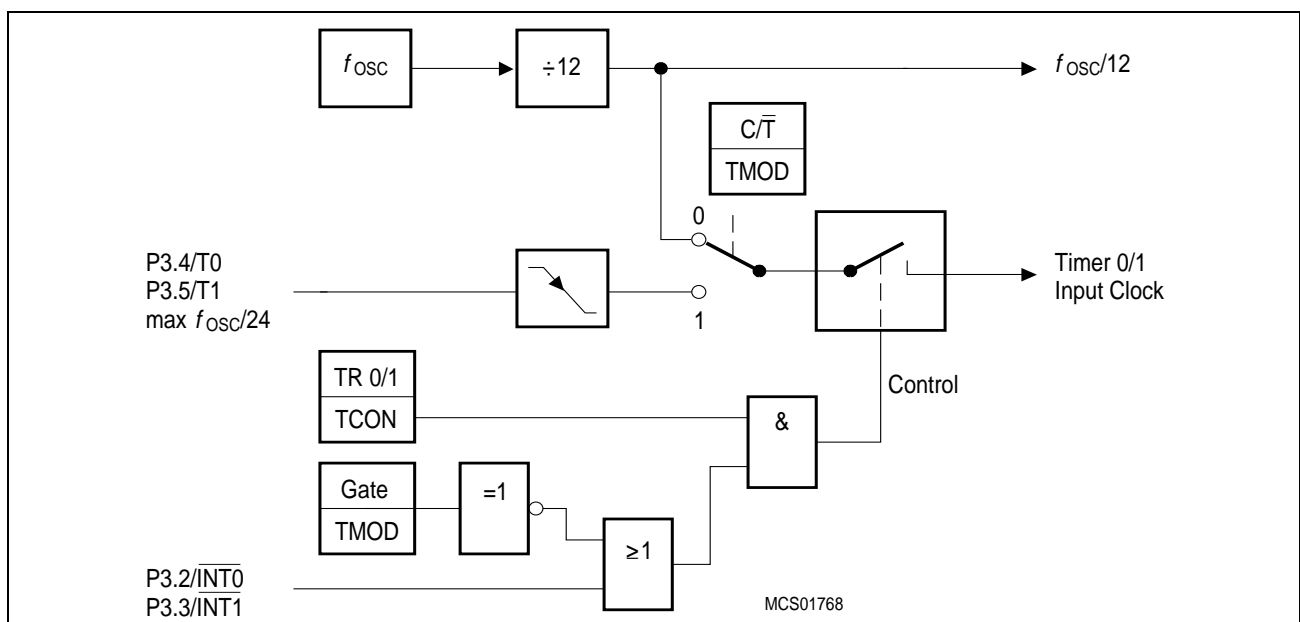


Figure 10 Timer/Counter 0 and 1 Input Clock Logic

Timer/Counter 2

Timer 2 is a 16-bit Timer/Counter with an up/down count feature. It can operate either as a timer or as an event counter. This is selected by bit $C/\overline{T2}$ of SFR T2CON. It has three operating modes as shown in **Table 5**.

Table 5 Timer/Counter 2 Operating Modes

| Mode | T2CON | | | T2MOD DCEN | T2CON EXEN | P1.1/ T2EX | Remarks | Input Clock | |
|--------------------------------|----------------------|------------|-----|---------------|---------------|---------------|--|--------------|-----------------------|
| | R×CLK or T×CLK | CP/ RL2 | TR2 | | | | | internal | external (P1.0/T2) |
| 16-bit Auto- reload | 0 | 0 | 1 | 0 | 0 | X | reload upon overflow | $f_{osc}/12$ | max $f_{osc}/24$ |
| | 0 | 0 | 1 | 0 | 1 | ↓ | reload trigger (falling edge) | | |
| | 0 | 0 | 1 | 1 | X | 0 | Down counting | | |
| | 0 | 0 | 1 | 1 | X | 1 | Up counting | | |
| 16-bit Cap- ture | 0 | 1 | 1 | X | 0 | X | 16 bit Timer/ Counter (only up-counting) | $f_{osc}/12$ | max $f_{osc}/24$ |
| | 0 | 1 | 1 | X | 1 | ↓ | capture TH2, TL2 → RC2H, RC2L | | |
| Baud Rate Gene- rator | 1 | X | 1 | X | 0 | X | no overflow interrupt request (TF2) | $f_{osc}/2$ | max $f_{osc}/24$ |
| | 1 | X | 1 | X | 1 | ↓ | extra external interrupt ("Timer 2") | | |
| off | X | X | 0 | X | X | X | Timer 2 stops | – | – |

Note: ↓ =  falling edge

Capture/Compare Unit

The Capture/Compare Unit (CCU) of the C504 consists of a 16-bit 3-channel capture/compare unit (CAPCOM) and a 10-bit 1-channel compare unit (COMP). In compare mode, the CAPCOM unit provides two output signals per channel, which can have inverted signal polarity and non-overlapping pulse transitions. The COMP unit can generate a single PWM output signal and is further used to modulate the CAPCOM output signals. In capture mode, the value of the Compare Timer 1 is stored in the capture registers if a signal transition occurs at the pins CCx. **Figure 11** shows the block diagram of the CCU.

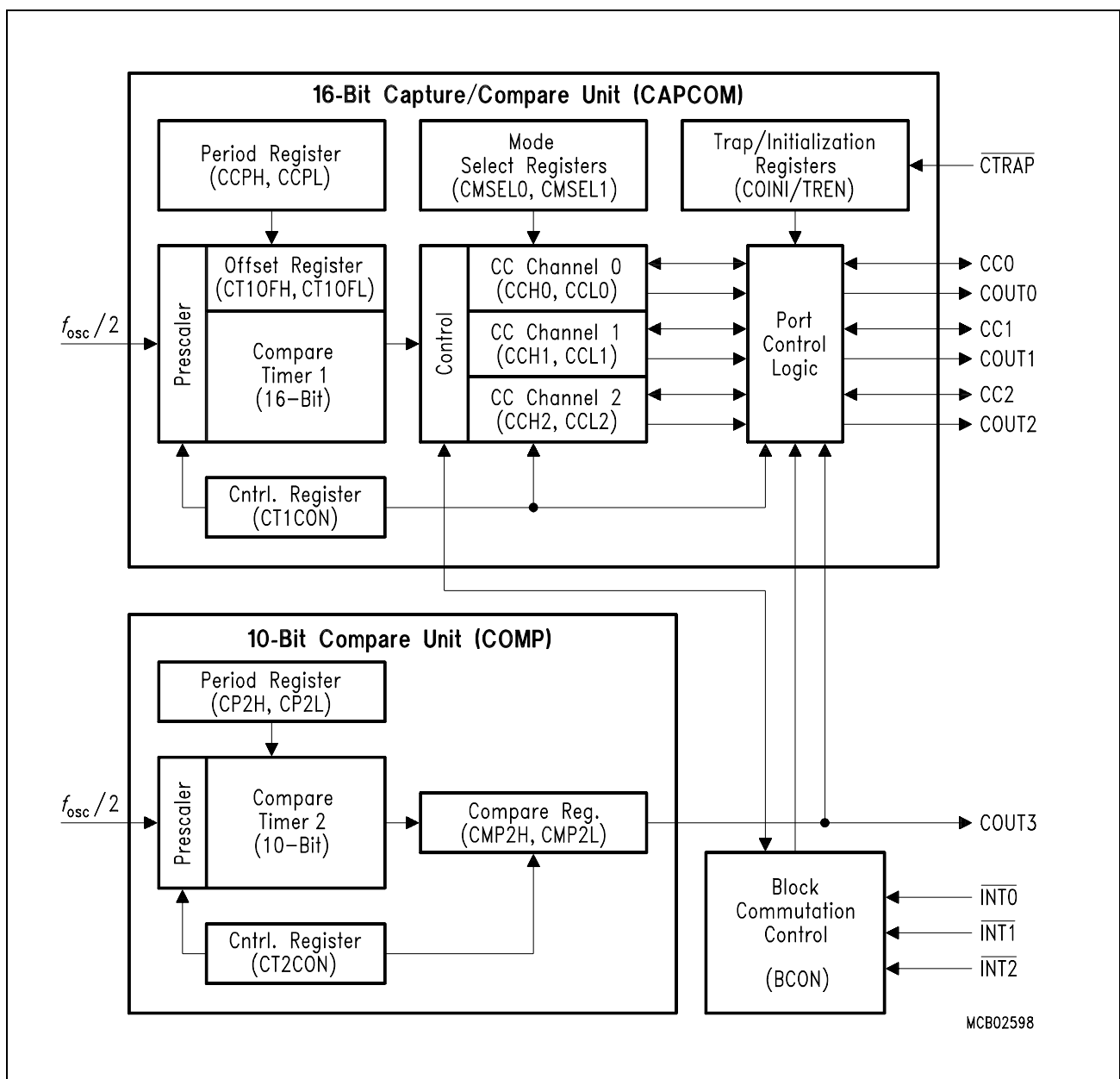


Figure 11 Block Diagram of the CCU

The Compare Timers 1 and 2 are free running, processor clock coupled 16-bit / 10-bit timers; each of which has a count rate with a maximum of $f_{OSC}/2$ up to $f_{OSC}/256$. The compare timer operations with its possible compare output signal waveforms are shown in **Figure 12**.

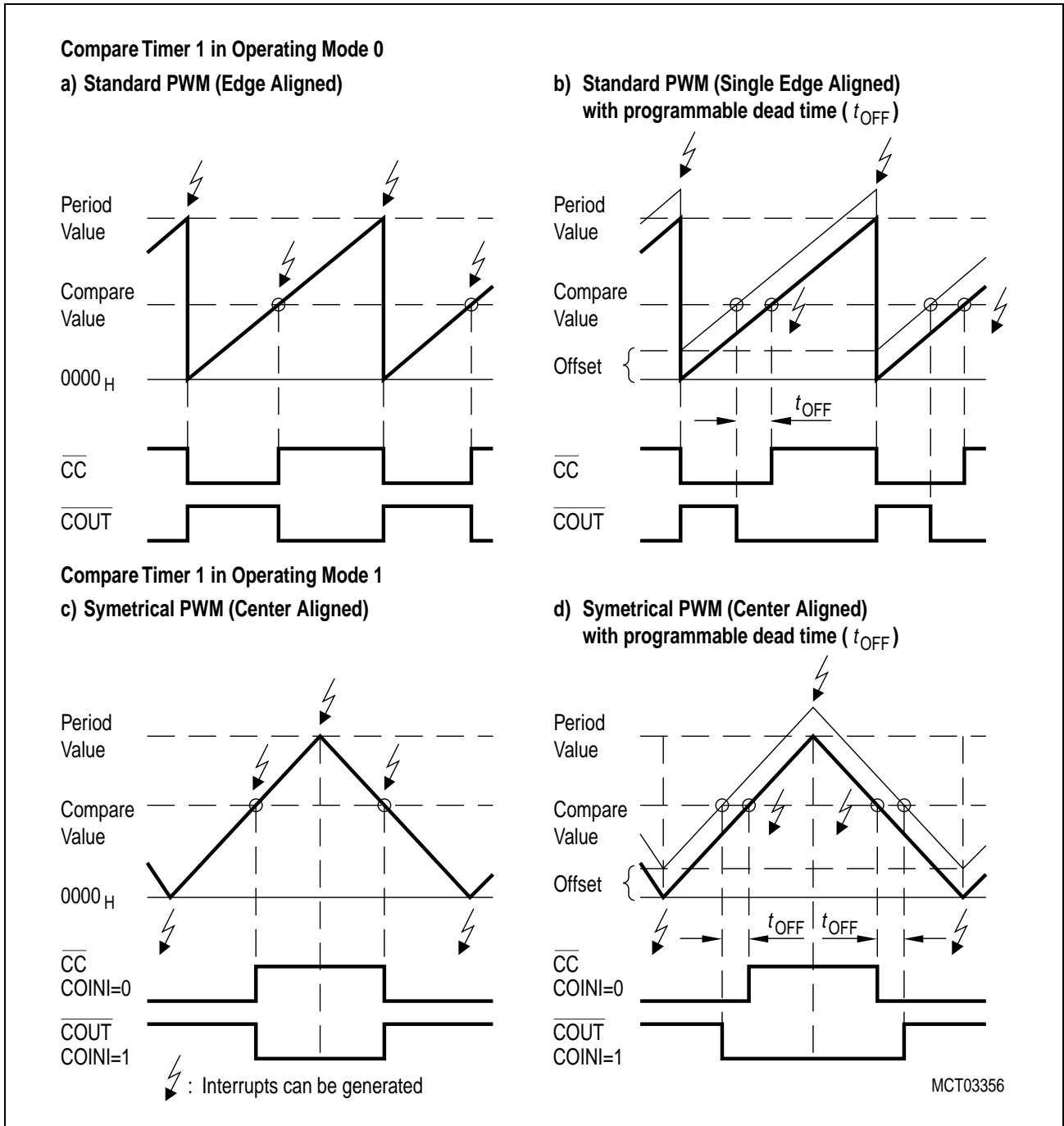


Figure 12 Basic Operating Modes of the CAPCOM Unit

Compare Timer 1 can be programmed for both operating modes while Compare Timer 2 works only in operating mode 0 with one output signal of selectable polarity at the pin COUT3.

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **Table 6**. The possible baud rates can be calculated using the formulas given in **Table 6**.

Table 6 USART Operating Modes

| Mode | SCON | | Baud Rate | Description |
|------|------|-----|------------------------------|---|
| | SM0 | SM1 | | |
| 0 | 0 | 0 | $f_{osc}/12$ | Serial data enters and exits through RxD. TxD outputs the shift clock. 8-bit are transmitted/received (LSB first) |
| 1 | 0 | 1 | Timer 1/2 overflow rate | 8-bit UART 10 bits are transmitted (through TxD) or received (RxD) |
| 2 | 1 | 0 | $f_{osc}/32$ or $f_{osc}/64$ | 9-bit UART 11 bits are transmitted (TxD) or received (RxD) |
| 3 | 1 | 1 | Timer 1/2 overflow rate | 9-bit UART Like mode 2 except the variable baud rate |

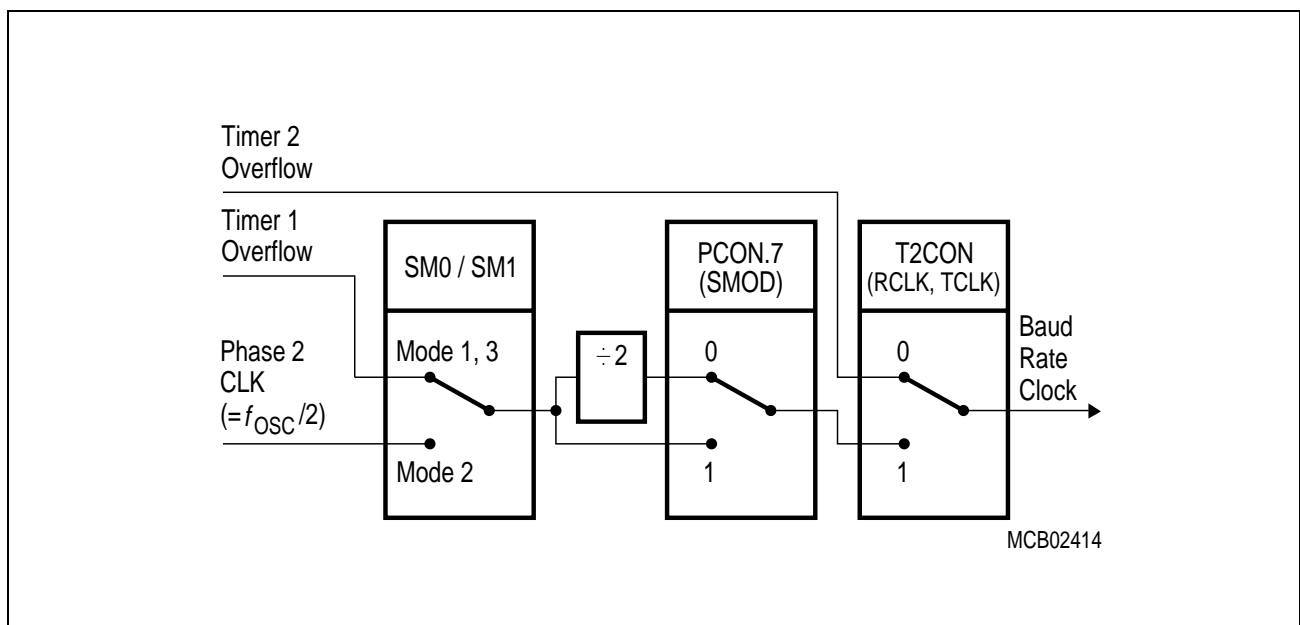


Figure 13 Baud Rate Generation for the Serial Interface

The possible baud rates can be calculated using the formulas given in **Table 7**.

Table 7 Formulas for Calculating Baud Rates

| Source of Baud Rate | Operating Mode | Baud Rate |
|---------------------------|---|---|
| Oscillator | 0 | $f_{OSC}/12$ |
| | 2 | $(2^{SMOD} \times f_{OSC})/64$ |
| Timer 1 (16-bit timer) | 1, 3 | $(2^{SMOD} \times \text{timer 1 overflow rate})/32$ |
| | (8-bit timer with 8-bit auto-reload) | $(2^{SMOD} \times f_{OSC})/(32 \times 12 \times (256-TH1))$ |
| Timer 2 | 1, 3 | $f_{OSC}/(32 \times (65536-(RC2H, RC2L)))$ |

10-Bit A/D Converter

The C504 has a high performance 8-channel 10-bit A/D converter using successive approximation technique for the conversion of analog input voltages. **Figure 14** shows the block diagram of the A/D Converter.

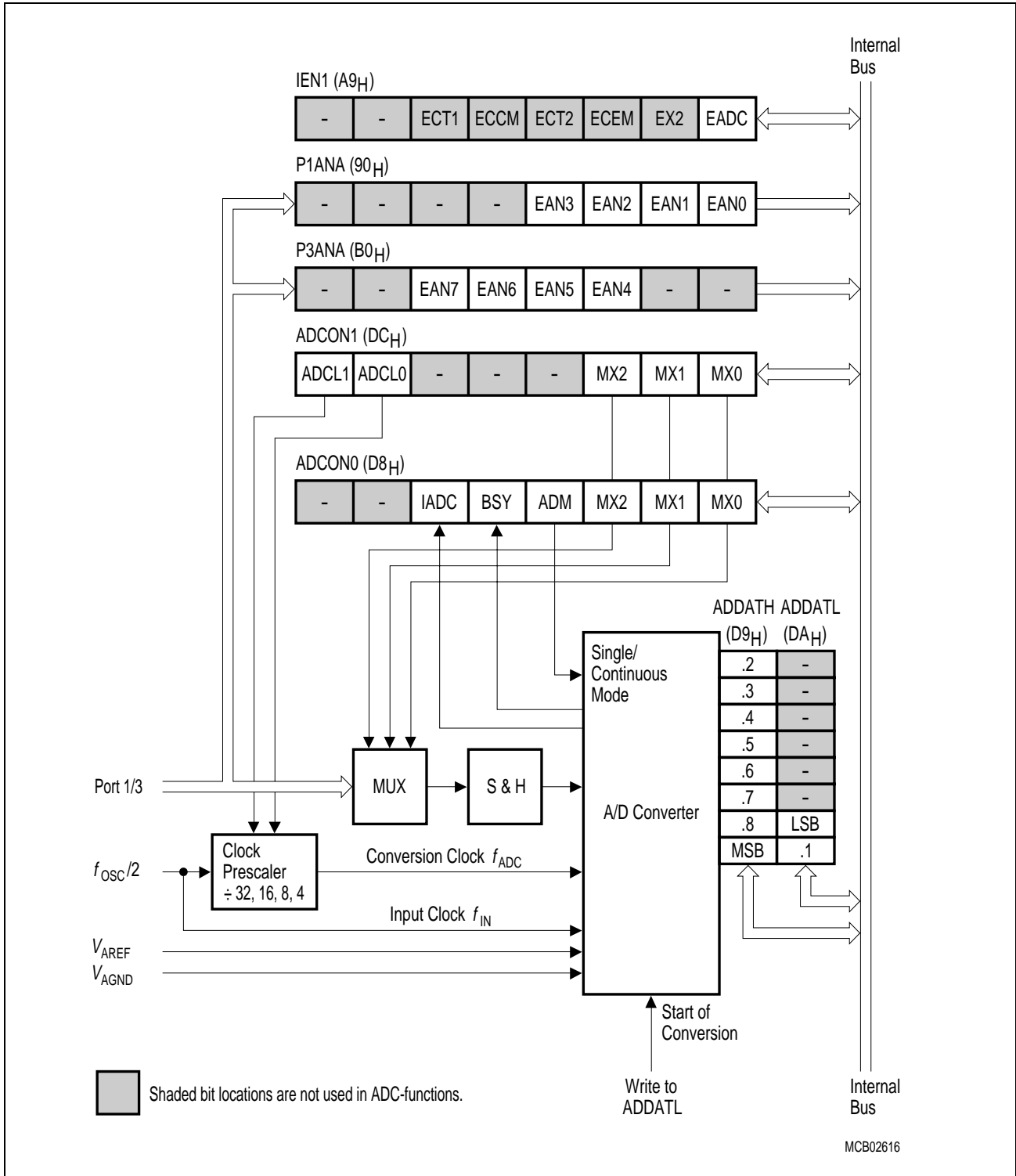


Figure 14 A/D Converter Block Diagram

The A/D Converter uses two clock signals for operation: the conversion clock f_{ADC} ($= 1/t_{ADC}$) and the input clock f_{IN} ($= 1/t_{IN}$). Both clock signals are derived from the C504 system clock f_{OSC} which is applied at the XTAL pins. The duration of an A/D conversion is a multiple of the period of the f_{IN} clock signal. The table in **Figure 15** shows the prescaler ratios and the resulting A/D conversion times which must be selected for typical system clock rates.

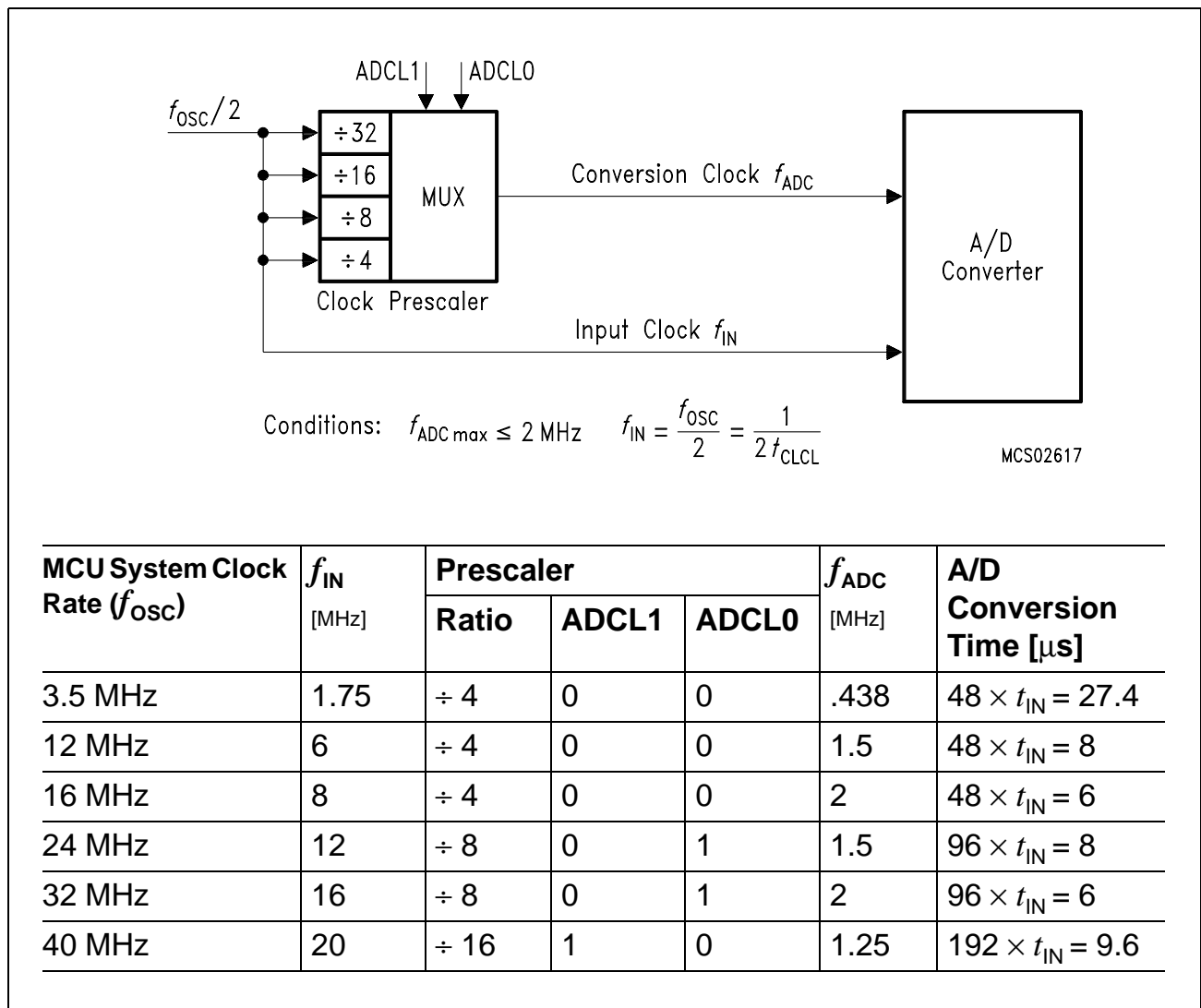


Figure 15 A/D Converter Clock Selection

The analog inputs are located at Port 1 and Port 3 (4 lines on each port). The corresponding Port 1 and Port 3 pins have a port structure, which allows the pins to be used either as digital I/Os or analog inputs. The analog input function of these mixed digital/analog port lines is selected via the registers P1ANA and P3ANA.

Interrupt System

The C504 provides 12 interrupt sources with two priority levels. **Figures 16 and 17** give a general overview of the interrupt sources and illustrate the interrupt request and control flags.

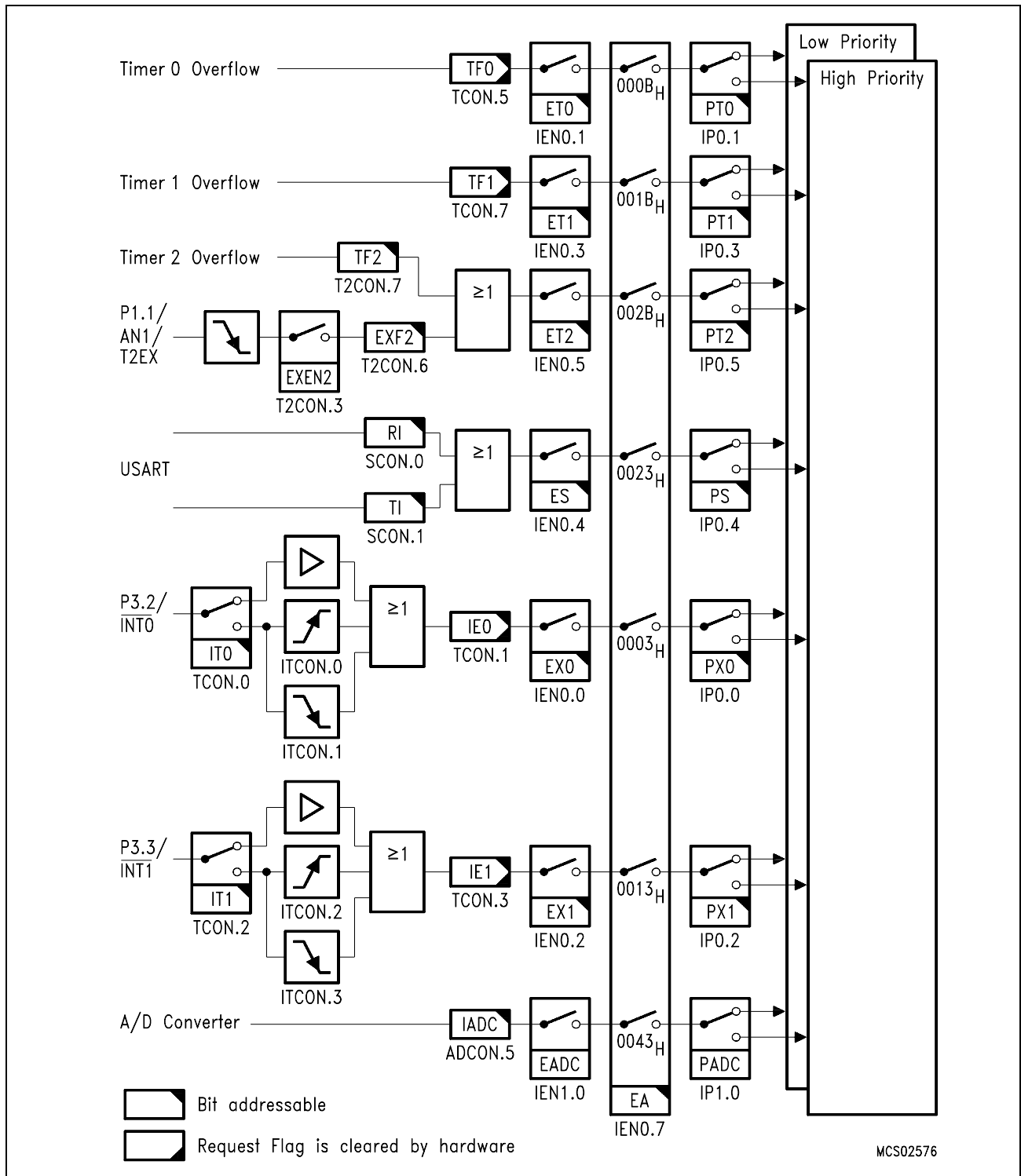


Figure 16 Interrupt Request Sources (Part 1)

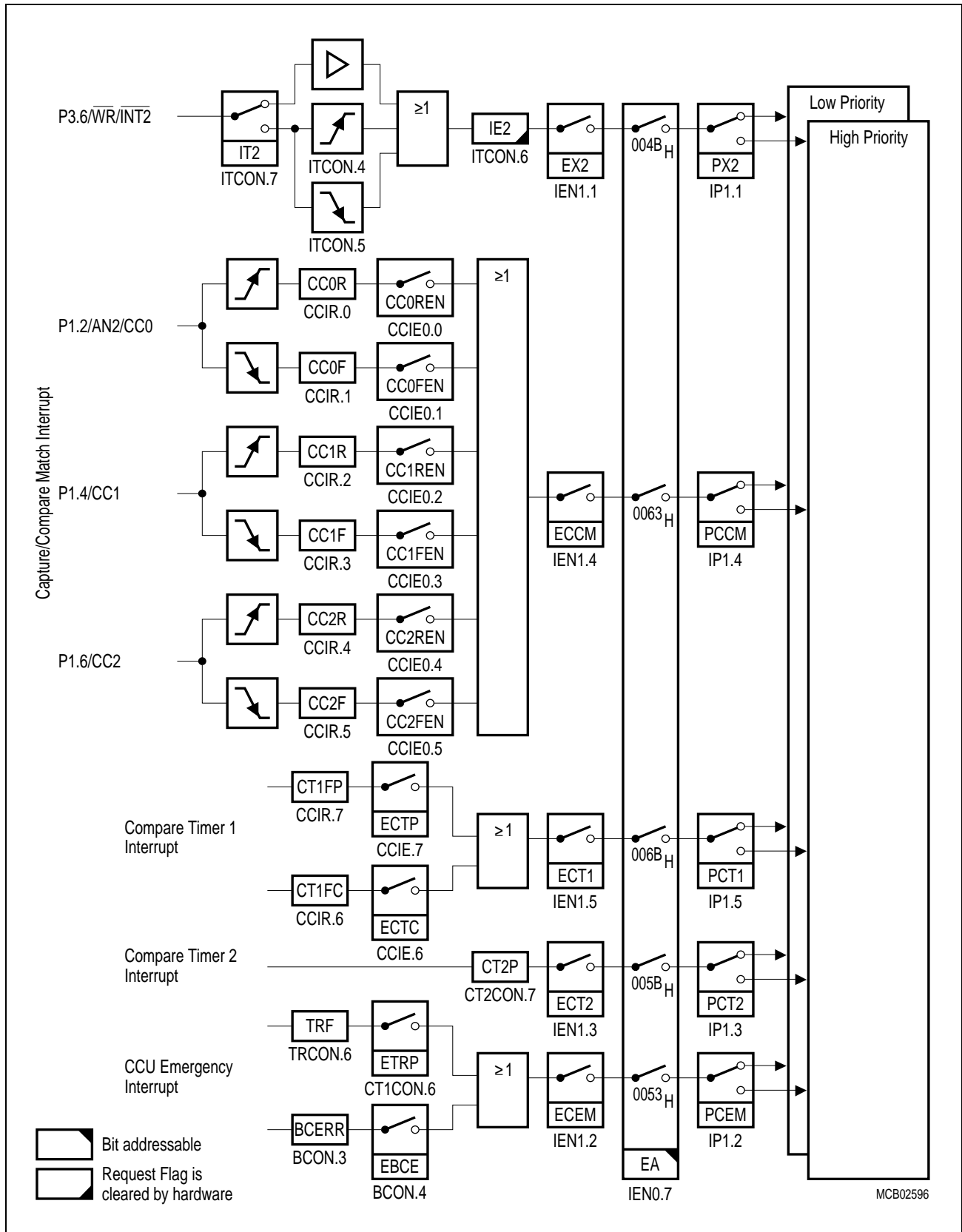


Figure 17 Interrupt Request Sources (Part 2)

Table 8 Interrupt Vector Addresses

| Request Flags | Interrupt Source | Vector Address |
|----------------------|---------------------------------|-------------------|
| IE0 | External interrupt 0 | 0003 _H |
| TF0 | Timer 0 interrupt | 000B _H |
| IE1 | External interrupt 1 | 0013 _H |
| TF1 | Timer 1 interrupt | 001B _H |
| RI + TI | Serial port interrupt | 0023 _H |
| TF2 + EXF2 | Timer 2 interrupt | 002B _H |
| IADC | A/D converter interrupt | 0043 _H |
| IE2 | External interrupt 2 | 004B _H |
| TRF, BCERR | CAPCOM emergency interrupt | 0053 _H |
| CT2P | Compare timer 2 interrupt | 005B _H |
| CC0F-CC2F, CC0R-CC2R | Capture/compare match interrupt | 0063 _H |
| CT1FP, CT1FC | Compare timer 1 interrupt | 006B _H |
| – | Power-down interrupt | 007B _H |

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt sources.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in **Table 9**.

Table 9 Interrupt Source Structure

| Interrupt Source | Priority | | | |
|--|----------------------|---------------------|---------------------|--|
| <table style="width: 100%; border: none;"> <tr> <td style="width: 33%; text-align: center;">High Priority</td> <td style="width: 33%; text-align: center;">→</td> <td style="width: 33%; text-align: center;">Low Priority</td> </tr> </table> | High Priority | → | Low Priority | |
| High Priority | → | Low Priority | | |
| External Interrupt 0 | High | | | |
| Timer 0 Interrupt | ↓ | | | |
| External Interrupt 1 | | | | |
| Timer 1 Interrupt | | | | |
| Serial Channel | | | | |
| Timer 2 Interrupt | | | | |
| Timer 2 Interrupt | | Low | | |

Fail Save Mechanisms

The C504 offers enhanced fail save mechanisms, which allow an automatic recovery from software or hardware failure.

- a programmable 15-bit Watchdog Timer
- Oscillator Watchdog

Programmable Watchdog Timer

The Watchdog Timer in the C504 is a 15-bit timer, which is incremented by a count rate of either $f_{CYCLE}/2$ or $f_{CYCLE}/32$ ($f_{CYCLE} = f_{OSC}/12$). Only the upper 7 bits of the 15-bit watchdog timer count value can be programmed. **Figure 18** shows the block diagram of the programmable Watchdog Timer.

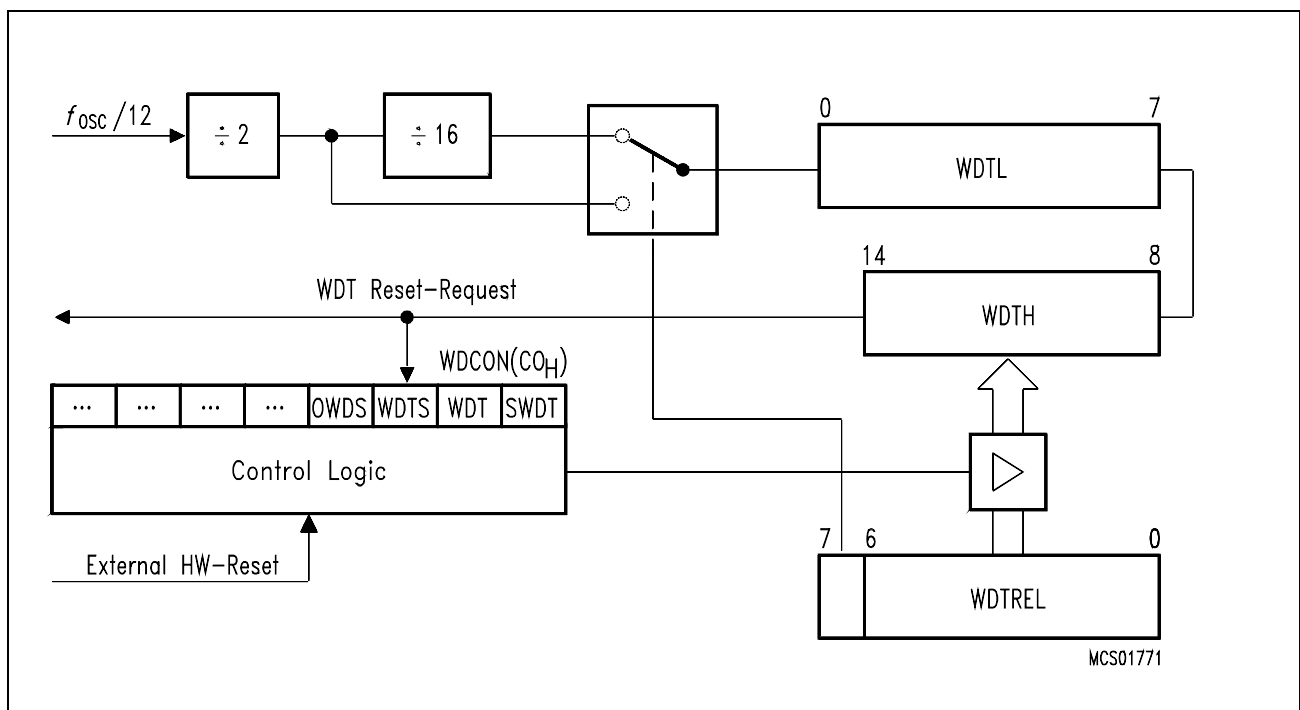


Figure 18 Block Diagram of the Programmable Watchdog Timer

The Watchdog Timer can be started by software (bit SWDT in SFR WDCON), but it cannot be stopped during active mode of the device. If the software fails to refresh the running Watchdog Timer, an internal reset will be initiated. The reset cause (external reset or reset caused by the watchdog) can be examined by software (status flag WDS in SFR WDCON is set). A refresh of the Watchdog Timer is done by setting bits WDT and SWDT (both in SFR WDCON) consecutively.

This double instruction sequence has been implemented to increase system security.

It must be noted, however, that the Watchdog Timer is halted during the idle mode and power down mode of the processor.

Oscillator Watchdog

The Oscillator Watchdog of the C504 serves for three functions:

- **Monitoring of the on-chip oscillator's function**

The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of an auxiliary RC oscillator, the internal clock is supplied by this RC oscillator and the C504 is brought into reset. If the failure condition disappears, the C504 executes a final reset phase of typically 1 ms in order to allow the oscillator to stabilize; then, the Oscillator Watchdog reset is released and the part starts program execution again.

- **Fast internal reset after power-on**

The oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. The Oscillator Watchdog unit also works identically to the monitoring function.

- **Control of external wake-up from software power-down mode**

When the software power-down mode is terminated by a low level at pin P3.2/ $\overline{\text{INT0}}$, the Oscillator Watchdog unit ensures that the microcontroller resumes operation (execution of the power-down wake-up interrupt) with the nominal clock rate. In the power-down mode, the RC oscillator and the on-chip oscillator are stopped. Both oscillators are started again when power-down mode is released. When the on-chip oscillator has a higher frequency than the RC oscillator, the microcontroller starts operation after a final delay of typically 1 ms in order to allow the on-chip oscillator to stabilize.

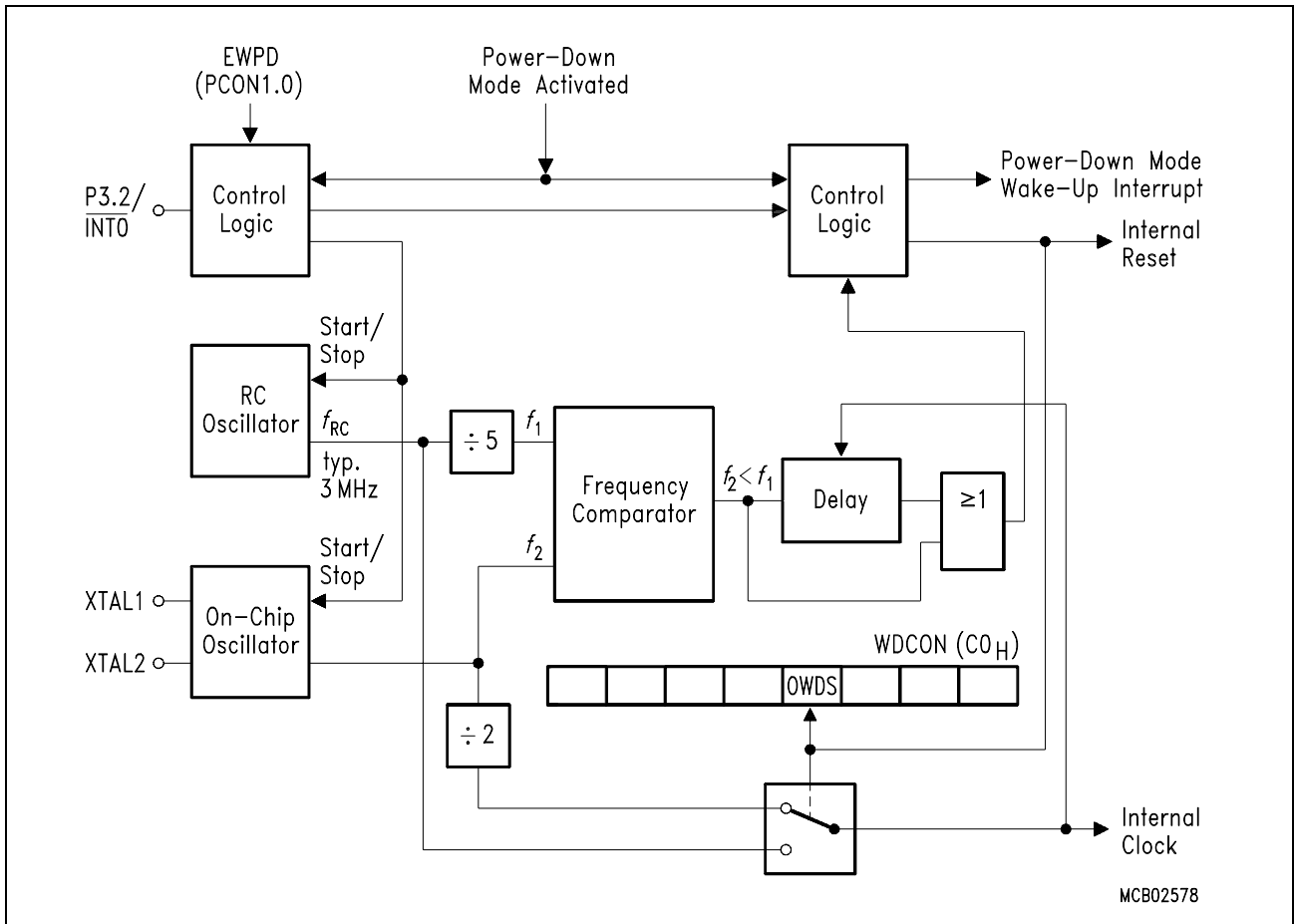


Figure 19 Block Diagram of the Oscillator Watchdog

Power Saving Modes

The C504 provides two power saving modes, the idle mode and the power down mode.

- In the **idle mode**, the oscillator of the C504 continues to run, but the CPU is gated off from the clock signal. However, the interrupt system, the serial port, the A/D Converter, and all timers with the exception of the Watchdog Timer, are further provided with the clock. The CPU status is preserved in its entirety: the stack pointer, program counter, program status word, accumulator, and all other registers maintain their data during idle mode.
- In the **power down** mode, the RC oscillator and the on-chip oscillator which operates with the XTAL pins are both stopped. Therefore all functions of the microcontroller are stopped and only the contents of the on-chip RAM, XRAM and the SFRs are maintained. The port pins, which are controlled by their port latches, output the values that are held by their SFRs.

Table 10 gives a general overview of the entry and exit procedures of the power saving modes.

Table 10 Power Saving Modes Overview

| Mode | Entering (2-Instruction Example) | Leaving by | Remarks |
|-----------------|---|---|---|
| Idle mode | ORL PCON, #01H ORL PCON, #20H | Occurrence of any enabled interrupt | CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with clock. |
| | | Hardware Reset | |
| Power Down mode | With external wake-up capability from power down enabled ORL SYSCON,#10H ORL PCON1,#80H ANL SYSCON,#0EFH ORL PCON,#02H ORL PCON,#40H | Hardware Reset | Oscillator is stopped; Contents of on-chip RAM and SFRs are maintained. |
| | | P3.2/ $\overline{\text{INT0}}$ goes low for at least 10 μs . It is desired that the pin be held at high level during the power down mode entry and up to the wake-up. | |
| | With external wake-up capability from power down disabled ORL PCON,#02H ORL PCON,#40H | Hardware Reset | |

If a power saving mode is terminated through an interrupt, including the external wake-up via P3.2/ $\overline{\text{INT0}}$, the microcontroller state (CPU, ports, peripherals) remains preserved. If it is terminated by a hardware reset, the microcontroller is reset to its default state.

In the power down mode of operation, V_{DD} can be reduced to minimize power consumption. It must be ensured, however, that V_{DD} is not reduced before the power down mode is invoked, and that V_{DD} is restored to its normal operating level, before the power down mode is terminated.

OTP Memory Operation (C504-2E only)

The C504-2E is the OTP version of the C504 microcontroller with a 16Kbyte one-time programmable (OTP) program memory. Fast programming cycles are achieved (1 byte in 100 μ s) with the C504-2E. Several levels of OTP memory protection can be selected as well.

To program the device, the C504-2E must be put into the programming mode. Typically, this is not done in-system, but in a special programming hardware. In the programming mode, the C504-2E operates as a slave device similar to an EPROM standalone memory device and must be controlled with address/data information, control lines, and an external 11.5 V programming voltage.

Figure 20 shows the pins of the C504-2E which are required for controlling of the OTP programming mode.

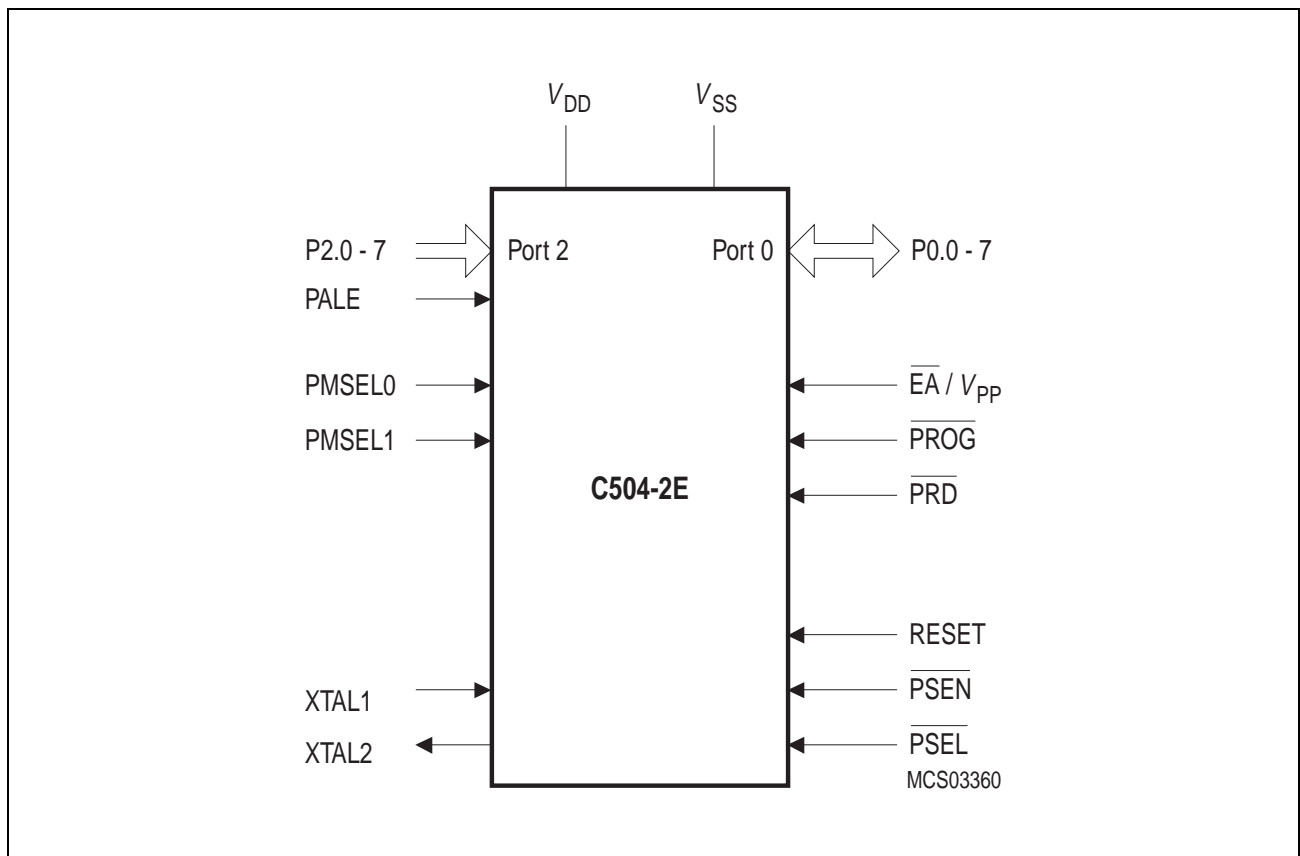


Figure 20 C504-2E Programming Mode Configuration

Pin Configuration in Programming Mode

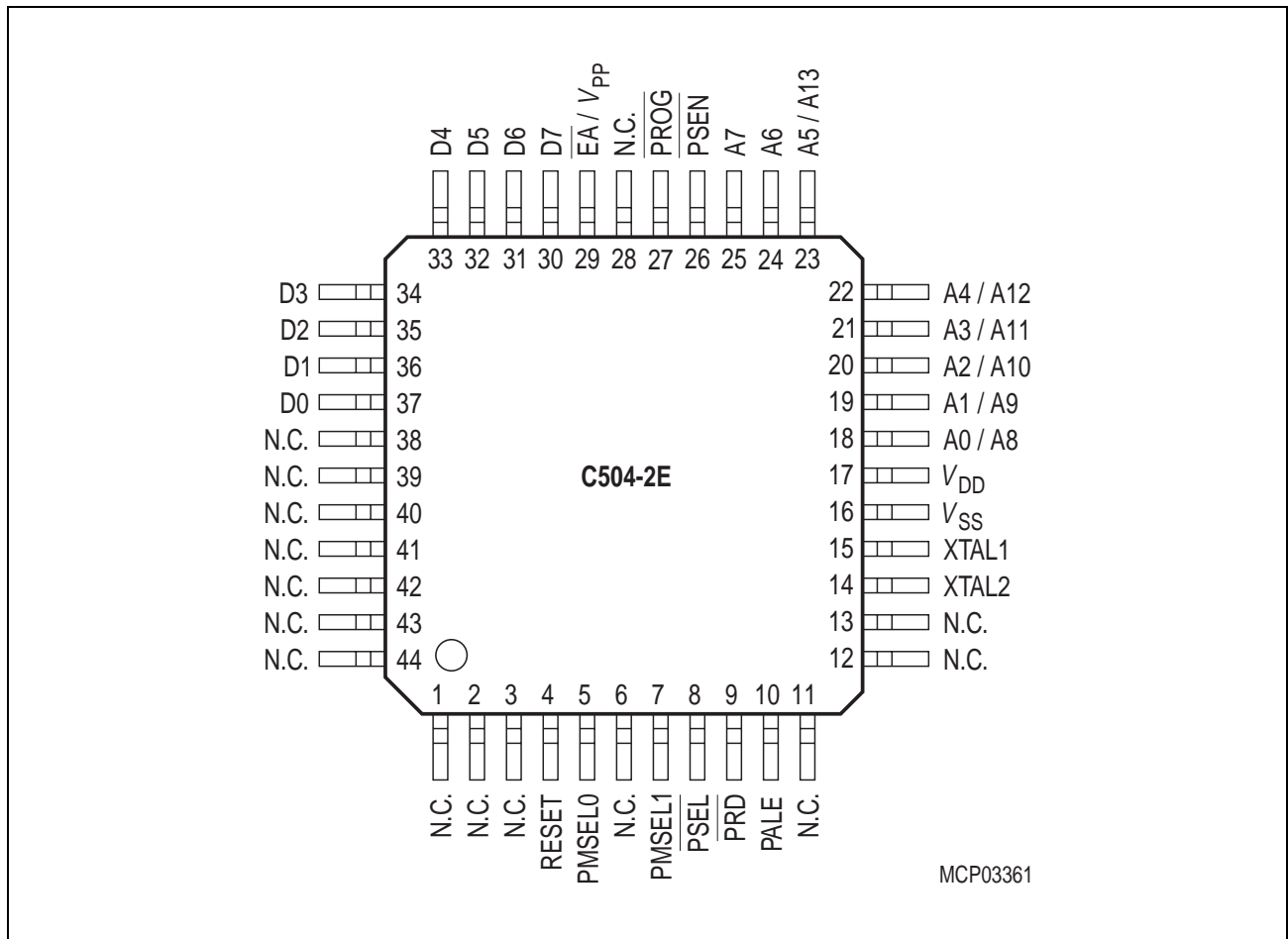


Figure 21 Pin Configuration of the C504-2E in Programming Mode (top view)

Pin Definitions

Table 11 contains the functional description of all C504-2E pins which are required for OTP memory programming.

Table 11 Pin Definitions and Functions of the C504-2E in Programming Mode

| Symbol | Pin No. | I/O | Function | | | | | | | | | | | | | | | |
|--------------------------|-----------|------------------------------|--|--------|--------|-------------|---|---|----------|---|---|--------------------|---|---|------------------------|---|---|------------------------------|
| | P-MQFP-44 | | | | | | | | | | | | | | | | | |
| RESET | 4 | I | <p>Reset This input must be at static “1” (active) level throughout the entire programming mode.</p> | | | | | | | | | | | | | | | |
| PMSEL0 PMSEL1 | 5 7 | I I | <p>Programming mode selection pins These pins are used to select the different access modes in programming mode. PMSEL1,0 must satisfy a setup time to the rising edge of PALE. When the logic level of PMSEL1,0 is changed, PALE must be at low level.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>PMSEL1</th> <th>PMSEL0</th> <th>Access Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>0</td> <td>1</td> <td>Read version bytes</td> </tr> <tr> <td>1</td> <td>0</td> <td>Program/read lock bits</td> </tr> <tr> <td>1</td> <td>1</td> <td>Program/read OTP memory byte</td> </tr> </tbody> </table> | PMSEL1 | PMSEL0 | Access Mode | 0 | 0 | Reserved | 0 | 1 | Read version bytes | 1 | 0 | Program/read lock bits | 1 | 1 | Program/read OTP memory byte |
| PMSEL1 | PMSEL0 | Access Mode | | | | | | | | | | | | | | | | |
| 0 | 0 | Reserved | | | | | | | | | | | | | | | | |
| 0 | 1 | Read version bytes | | | | | | | | | | | | | | | | |
| 1 | 0 | Program/read lock bits | | | | | | | | | | | | | | | | |
| 1 | 1 | Program/read OTP memory byte | | | | | | | | | | | | | | | | |
| $\overline{\text{PSEL}}$ | 8 | I | <p>Basic programming mode select This input is used for the basic programming mode selection and must be switched according to Figure 22.</p> | | | | | | | | | | | | | | | |
| $\overline{\text{PRD}}$ | 9 | I | <p>Programming mode read strobe This input is used for read access control for OTP memory read, version byte read, and lock bit read operations.</p> | | | | | | | | | | | | | | | |
| PALE | 10 | I | <p>Programming address latch enable PALE is used to latch the high address lines. The high address lines must satisfy a setup and hold time to/from the falling edge of PALE. PALE must be at low level when the logic level of PMSEL1,0 is changed.</p> | | | | | | | | | | | | | | | |
| XTAL2 | 14 | O | <p>XTAL2 Output of the inverting oscillator amplifier.</p> | | | | | | | | | | | | | | | |

Table 11 Pin Definitions and Functions of the C504-2E in Programming Mode (cont'd)

| Symbol | Pin No. | I/O | Function |
|-------------------------------|--------------------------|-----|---|
| | P-MQFP-44 | | |
| XTAL1 | 15 | I | XTAL1 Input to the oscillator amplifier. |
| V_{SS} | 16 | – | Ground (0 V) must be applied in programming mode. |
| V_{DD} | 17 | – | Power Supply (+ 5 V) must be applied in programming mode. |
| P2.0 - P2.7 | 18 - 25 | I | Address lines P2.0 - P2.7 are used as multiplexed address input lines A0 - A7 and A8 - A13. A8 - A13 must be latched with PALE. |
| $\overline{\text{PSEN}}$ | 26 | I | Program store enable This input must be at static “0” level during the whole programming mode. |
| $\overline{\text{PROG}}$ | 27 | I | Programming mode write strobe This input is used in programming mode as a write strobe for OTP memory program and lock bit write operations. During basic programming mode selection, a low level must be applied to PROG. |
| $\overline{\text{EA}}/V_{PP}$ | 29 | – | Programming Voltage This pin must be held at 11.5 V (V_{PP}) during programming of an OTP memory byte or lock bit. During an OTP memory read operation, this pin must be at V_{IH} . This pin is also used for basic programming mode selection. For basic programming mode selection, a low level must be applied. |
| P0.7 - P0.0 | 30-37 | I/O | Data lines In programming mode, data bytes are transferred via the bidirectional D7 - D0 data lines which are located at Port 0. |
| N.C. | 1-3, 6, 11-13, 28, 38-44 | – | Not Connected These pins should not be connected in programming mode. |

Programming Mode Selection

The selection for the OTP programming mode can be separated into two different parts:

- Basic programming mode selection
- Access mode selection

With basic programming mode selection, the device is put into the mode in which it is possible to access the OTP memory through the programming interface logic. Further, after selection of the basic programming mode, OTP memory accesses are executed by using one of the access modes. These access modes are OTP memory byte program/read, version byte read, and program/read lock byte operations.

The basic programming mode selection scheme is shown in **Figure 22**.

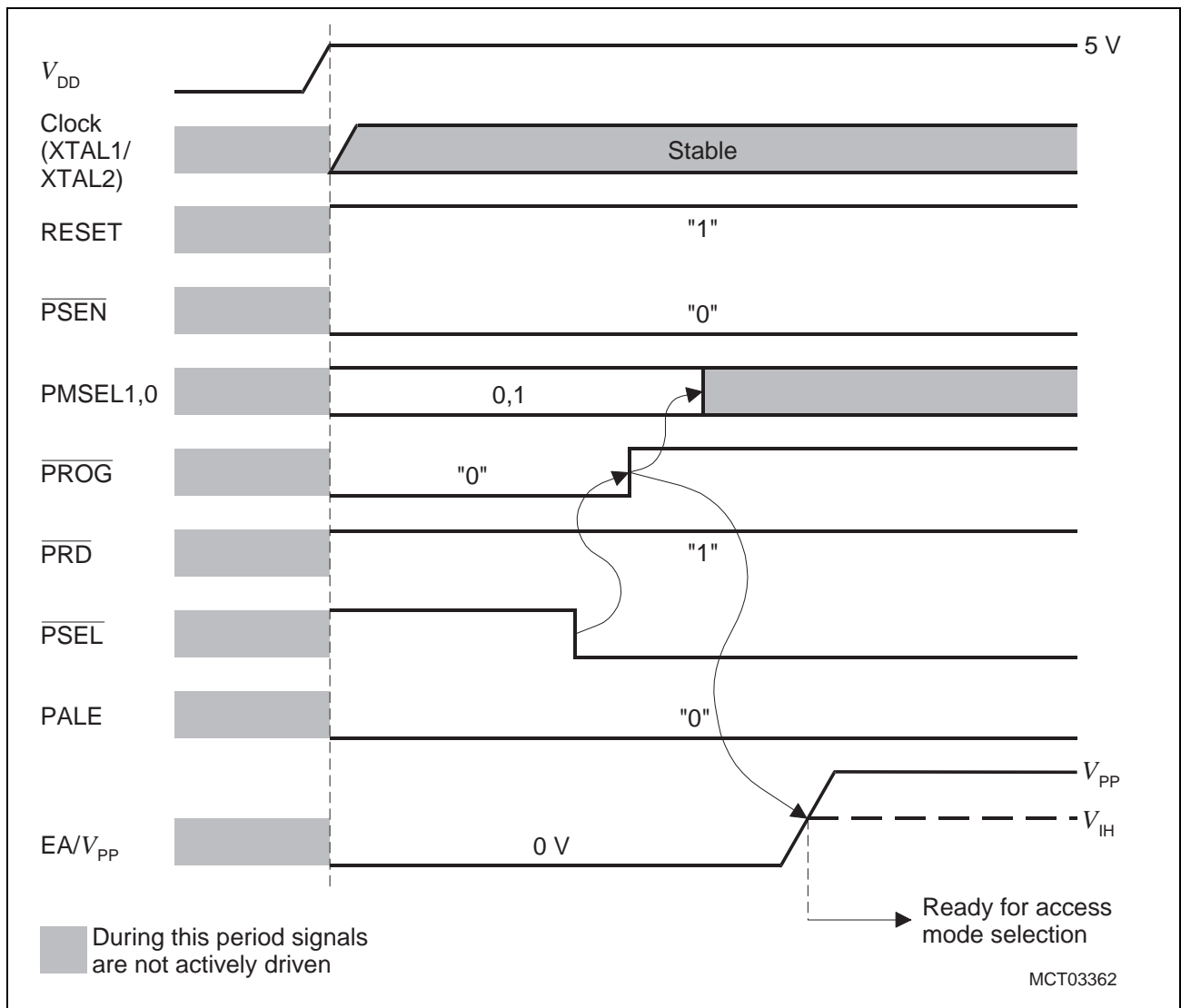







Figure 22 Basic Programming Mode Selection

Table 12 Access Modes Selection

| Access Mode | EA/ V _{PP} | PROG | PRD | PMSEL | | Address (Port 2) | Data (Port 0) |
|-------------------------|------------------------|---|---|-------|---|-------------------------------|---------------------------------|
| | | | | 1 | 0 | | |
| Program OTP memory byte | V _{PP} |  | H | H | H | A0 - A7 A8 - A15 | D0 - D7 |
| Read OTP memory byte | V _{IH} | H |  | | | | |
| Program OTP lock bits | V _{PP} |  | H | H | L | – | D1,D0 see Table 13 |
| Read OTP lock bits | V _{IH} | H |  | | | | |
| Read OTP version byte | V _{IH} | H |  | L | H | Byte addr. of version byte | D0 - D7 |

Lock Bits Programming / Read

The C504-2E has two programmable lock bits which, when programmed according to **Table 13**, provide four levels of protection for the on-chip OTP code memory.

Table 13 Lock Bit Protection Types

| Lock Bits | | Protection Level | Protection Type |
|-----------|----|------------------|---|
| D1 | D0 | | |
| 1 | 1 | Level 0 | The OTP lock feature is disabled. During normal operation of the C504-2E, the state of the EA pin is not latched on reset. |
| 1 | 0 | Level 1 | During normal operation of the C504-2E, MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. EA is sampled and latched on reset. An OTP memory read operation is only possible according to ROM/OTP verification mode 2. Further programming of the OTP memory is disabled (reprogramming security). |
| 0 | 1 | Level 2 | Same as level 1, but also OTP memory read operation using ROM verification mode 2 is disabled. |
| 0 | 0 | Level 3 | Same as level 2; but additionally external code execution by setting EA = low during normal operation of the C504-2E is no more possible. External code execution, which is initiated by an internal program (e.g. by an internal jump instruction above the ROM boundary), is still possible. |

Note: A '1' means that the lock bit is unprogrammed; a '0' means that lock bit is programmed.

Version Bytes

The C504-2E and C504-2R provide three version bytes at mapped address locations FC_H , FD_H , and FE_H . The information stored in the version bytes, is defined by the mask of each microcontroller step. Therefore, the version bytes can be read but not written. The three version bytes hold information as manufacturer code, device type, and stepping code.

The steppings of the C504 contain the following version byte information:

Table 14 **Content of Version Bytes**

| Stepping | Version Byte 0, VR0 (mapped addr. FC_H) | Version Byte 1, VR1 (mapped addr. FD_H) | Version Byte 2, VR2 (mapped addr. FE_H) |
|-----------------------|---|---|---|
| C504-2R AC-Step | $C5_H$ | 04_H | 01_H |
| C504-2E ES-AA-Step | $C5_H$ | 84_H | 01_H |
| C504-2E ES-BB-Step | $C5_H$ | 84_H | 04_H |
| C504-2E CA-Step | $C5_H$ | 84_H | 09_H |

Future steppings of the C504 will typically have a different value for version byte 2.

Absolute Maximum Ratings

| Parameter | Symbol | Limit Values | | Unit | Notes |
|--|------------|--------------|----------------|------|-------|
| | | min. | max. | | |
| Storage temperature | T_{ST} | - 65 | 150 | °C | - |
| Voltage on V_{DD} pins with respect to ground (V_{SS}) | V_{DD} | - 0.5 | 6.5 | V | - |
| Voltage on any pin with respect to ground (V_{SS}) | V_{IN} | - 0.5 | $V_{DD} + 0.5$ | V | - |
| Input current on any pin during overload condition | - | - 10 | 10 | mA | - |
| Absolute sum of all input currents during overload condition | - | - | 100 mA | mA | - |
| Power dissipation | P_{DISS} | - | 1 | W | - |

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

| Parameter | Symbol | Limit Values | | Unit | Notes |
|--------------------------|------------|----------------|----------------|------|-------|
| | | min. | max. | | |
| Supply voltage | V_{DD} | 4.25 | 5.5 | V | - |
| Ground voltage | V_{SS} | 0 | | V | - |
| Ambient temperature | | | | °C | - |
| SAB-C504 | T_A | 0 | 70 | | |
| SAF-C504 | T_A | - 40 | 85 | | |
| SAK-C504 | T_A | - 40 | 125 | | |
| Analog reference voltage | V_{AREF} | 4 | $V_{DD} + 0.1$ | V | - |
| Analog ground voltage | V_{AGND} | $V_{SS} - 0.1$ | $V_{SS} + 0.2$ | V | - |
| Analog input voltage | V_{AIN} | V_{AGND} | V_{AREF} | V | - |
| CPU clock | f_{CPU} | 1.75 | 20 | MHz | - |

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C504 and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (Controller Characteristics):

The logic of the C504 will provide signals with the respective characteristics.

SR (System Requirement):

The external system must provide signals with the respective characteristics to the C504.

DC Characteristics

(Operating Conditions apply)

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|--------------|-----------------------|-----------------------|------|--|
| | | min. | max. | | |
| Input low voltage (except \overline{EA} , RESET, CTRAP) | V_{IL} SR | - 0.5 | $0.2 V_{DD}$ - 0.1 | V | - |
| Input low voltage (\overline{EA}) | V_{IL1} SR | - 0.5 | $0.2 V_{DD}$ - 0.3 | V | - |
| Input low voltage (RESET, CTRAP) | V_{IL2} SR | - 0.5 | $0.2 V_{DD} +$ 0.1 | V | - |
| Input high voltage (except XTAL1, RESET and CTRAP) | V_{IH} SR | $0.2 V_{DD} +$ 0.9 | $V_{DD} + 0.5$ | V | ¹⁾ |
| Input high voltage to XTAL1 | V_{IH1} SR | $0.7 V_{DD}$ | $V_{DD} + 0.5$ | V | - |
| Input high voltage to RESET and CTRAP | V_{IH2} SR | $0.6 V_{DD}$ | $V_{DD} + 0.5$ | V | - |
| Output low voltage (Ports 1, 2, 3, COUT3) | V_{OL} CC | - | 0.45 | V | $I_{OL} = 1.6 \text{ mA}^{1)}$ |
| Output low voltage (Port 0, ALE, PSEN) | V_{OL1} CC | - | 0.45 | V | $I_{OL} = 3.2 \text{ mA}^{1)}$ |
| Output high voltage (Ports 1, 2, 3) | V_{OH} CC | 2.4 $0.9 V_{DD}$ | - - | V | $I_{OH} = - 80 \mu\text{A}$ $I_{OH} = - 10 \mu\text{A}$ |
| Output high voltage (Ports 1, 3 pins in push-pull mode and COUT3) | V_{OH1} CC | $0.9 V_{DD}$ | - | V | $I_{OH} = - 800 \mu\text{A}$ |

DC Characteristics (cont'd)
 (Operating Conditions apply)

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|--------------|---------------------|---------|---------|---|
| | | min. | max. | | |
| Output high voltage (Port 0 in external bus mode, ALE, PSEN) | V_{OH2} CC | 2.4 $0.9 V_{DD}$ | – – | V | $I_{OH} = -800 \mu A^{2)}$ $I_{OH} = -80 \mu A^{2)}$ |
| Logic 0 input current (Ports 1, 2, 3) | I_{IL} SR | – 10 | – 50 | μA | $V_{IN} = 0.45 V$ |
| Logical 1-to-0 transition current (Ports 1, 2, 3) | I_{TL} SR | – 65 | – 650 | μA | $V_{IN} = 2 V$ |
| Input leakage current (Port 0, \overline{EA}) | I_{LI} CC | – | ± 1 | μA | $0.45 < V_{IN} < V_{DD}$ |
| Pin capacitance | C_{IO} CC | – | 10 | pF | $f_c = 1 MHz,$ $T_A = 25 ^\circ C$ |
| Overload current | I_{OV} SR | – | ± 5 | mA | ^{7) 8)} |
| Programming voltage (C504-2E) | V_{PP} SR | 10.9 | 12.1 | V | $11.5 V \pm 5\%^{10)}$ |

Power Supply Current

| Parameter | | | Sym- bol | Limit Values | | Unit | Test Condition |
|--|---------|--------|-------------|--------------------|--------------------|---------|-------------------------------|
| | | | | typ. ⁸⁾ | max. ⁹⁾ | | |
| Active mode | C504-2R | 24 MHz | I_{DD} | 27.4 | 35.9 | mA | ⁴⁾ |
| | | 40 MHz | I_{DD} | 43.1 | 57.2 | mA | |
| | C504-2E | 24 MHz | I_{DD} | 20.9 | 27.9 | mA | |
| | | 40 MHz | I_{DD} | 31.0 | 41.5 | mA | |
| Idle mode | C504-2R | 24 MHz | I_{DD} | 14.6 | 19.3 | mA | ⁵⁾ |
| | | 40 MHz | I_{DD} | 22.4 | 31.3 | mA | |
| | C504-2E | 24 MHz | I_{DD} | 12.3 | 16.1 | mA | |
| | | 40 MHz | I_{DD} | 16.1 | 20.9 | mA | |
| Power-down mode | C504-2R | | I_{PD} | 1 | 30 | μA | $V_{DD} = 2 \dots 5.5 V^{3)}$ |
| | C504-2E | | I_{PD} | 35 | 60 | μA | |
| At \overline{EA}/V_{PP} in prog. mode | C504-2E | | I_{DDP} | – | 30 | mA | – |

Notes:

- 1) Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and Port 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt-trigger, or use an address latch with a Schmitt-trigger strobe input.
- 2) Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and \overline{PSEN} to momentarily fall below the 0.9 V_{DD} specification when the address lines are stabilizing.
- 3) I_{DD} (power-down mode) is measured under following conditions:
 $\overline{EA} = \text{Port 0} = V_{DD}$; $\text{RESET} = V_{SS}$; $\text{XTAL2} = \text{N.C.}$; $\text{XTAL1} = V_{SS}$; $V_{AGND} = V_{SS}$; all other pins are disconnected.
- 4) I_{DD} (active mode) is measured with:
 XTAL1 driven with t_{CLCH} , $t_{CHCL} = 5 \text{ ns}$, $V_{IL} = V_{SS} + 0.5 \text{ V}$, $V_{IH} = V_{DD} - 0.5 \text{ V}$; $\text{XTAL2} = \text{N.C.}$;
 $\overline{EA} = \text{Port 0} = \text{Port 1} = \text{RESET} = V_{DD}$; all other pins are disconnected. I_{DD} would be slightly higher if a crystal oscillator is used (appr. 1 mA).
- 5) I_{DD} (idle mode) is measured with all output pins disconnected and with all peripherals disabled;
 XTAL1 driven with t_{CLCH} , $t_{CHCL} = 5 \text{ ns}$, $V_{IL} = V_{SS} + 0.5 \text{ V}$, $V_{IH} = V_{DD} - 0.5 \text{ V}$; $\text{XTAL2} = \text{N.C.}$;
 $\text{RESET} = \overline{EA} = V_{SS}$; $\text{Port 0} = V_{DD}$; all other pins are disconnected;
- 6) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD} + 0.5 \text{ V}$ or $V_{OV} < V_{SS} - 0.5 \text{ V}$). The supply voltage V_{DD} and V_{SS} must remain within the specified limits. The absolute sum of input currents on all port pins may not exceed 50 mA.
- 7) Not 100 % tested, guaranteed by design characterization.
- 8) The typical I_{DD} values are periodically measured at $T_A = +25 \text{ }^\circ\text{C}$ and $V_{DD} = 5 \text{ V}$ but not 100% tested.
- 9) The maximum I_{DD} values are measured under worst case conditions ($T_A = 0 \text{ }^\circ\text{C}$ or $-40 \text{ }^\circ\text{C}$ and $V_{DD} = 5.5 \text{ V}$)
- 10) This V_{PP} specification is valid for devices with version byte 2 = 02H or higher. Devices with version byte 2 = 01H must be programmed with $V_{PP} = 12 \text{ V} \pm 5\%$.
- 11) For the C504-2E ES-AA-step the V_{IH} min. for \overline{EA} is 0.8 V_{DD} .

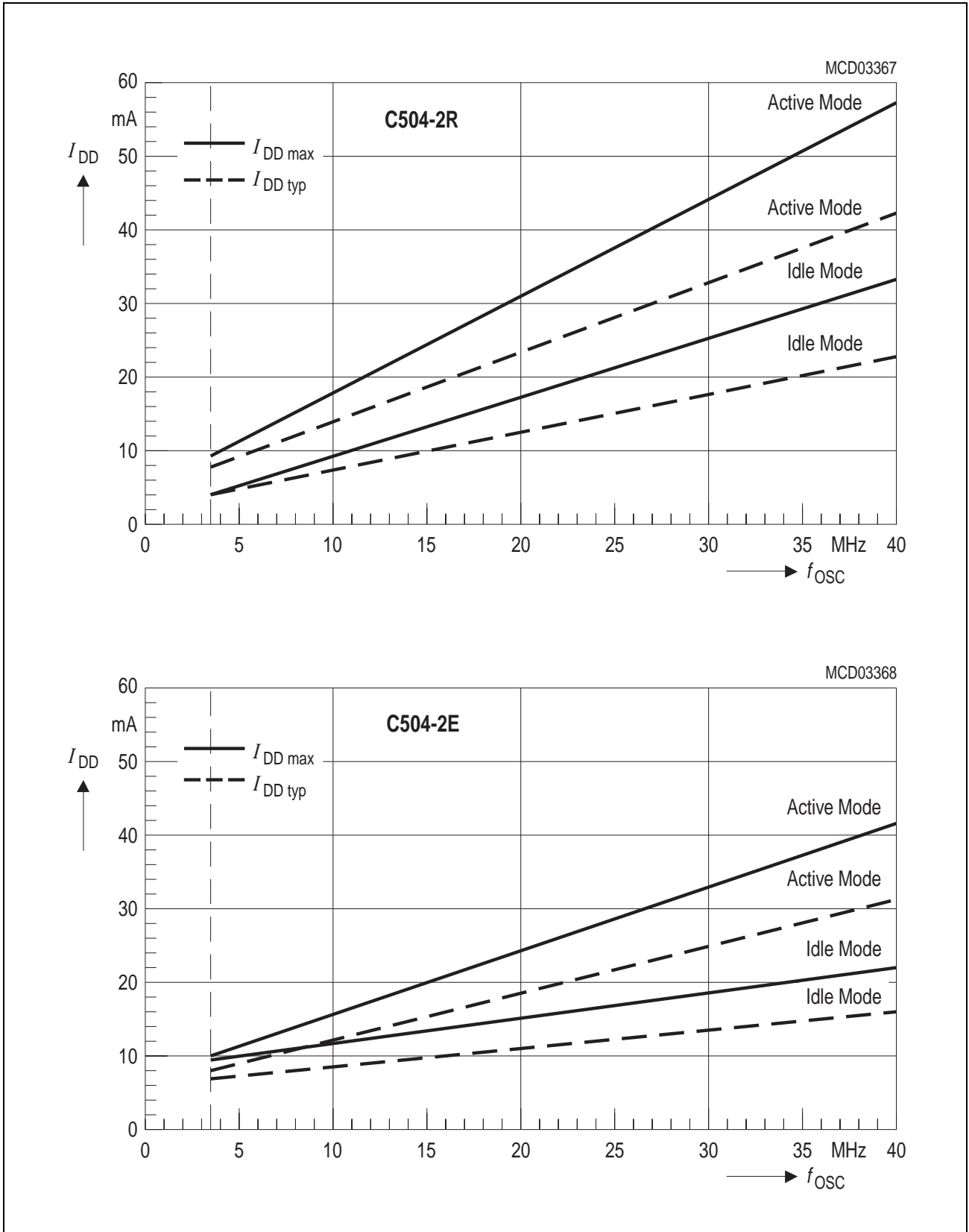


Figure 23 IDD Diagram

Power Supply Current Calculation Formulas

| Parameter | | Symbol | Formula |
|-------------|---------|--------------------------------|---|
| Active mode | C504-2R | $I_{DD\ typ}$ $I_{DD\ max}$ | $0.98 \times f_{OSC} + 3.9$ $1.33 \times f_{OSC} + 4.0$ |
| | C504-2E | $I_{DD\ typ}$ $I_{DD\ max}$ | $0.63 \times f_{OSC} + 5.75$ $0.85 \times f_{OSC} + 7.5$ |
| Idle mode | C504-2R | $I_{DD\ typ}$ $I_{DD\ max}$ | $0.51 \times f_{OSC} + 2.35$ $0.75 \times f_{OSC} + 1.3$ |
| | C504-2E | $I_{DD\ typ}$ $I_{DD\ max}$ | $0.24 \times f_{OSC} + 6.5$ $0.30 \times f_{OSC} + 8.86$ |

Note: f_{osc} is the oscillator frequency in MHz. I_{DD} values are given in mA.

A/D Converter Characteristics

(Operating Conditions apply)

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|---------------|--------------|--|------------|--|
| | | min. | max. | | |
| Analog input voltage | V_{AIN} SR | V_{AGND} | V_{AREF} | V | 1) |
| Sample time | t_S CC | – | $64 \times t_{IN}$ $32 \times t_{IN}$ $16 \times t_{IN}$ $8 \times t_{IN}$ | ns | Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 ²⁾ |
| Conversion cycle time | t_{ADCC} CC | – | $384 \times t_{IN}$ $192 \times t_{IN}$ $96 \times t_{IN}$ $48 \times t_{IN}$ | ns | Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 ³⁾ |
| Total unadjusted error | T_{UE} CC | – | ± 2 | LSB | $V_{SS} + 0.5\ V \leq V_{IN} \leq V_{DD} - 0.5\ V$ ⁴⁾ |
| | | – | ± 4 | LSB | $V_{SS} < V_{IN} < V_{SS} + 0.5\ V$ $V_{DD} - 0.5\ V < V_{IN} < V_{DD}$ ⁴⁾ |
| Internal resistance of reference voltage source | R_{AREF} SR | – | $t_{ADC}/250$ – 0.25 | k Ω | t_{ADC} in [ns] ^{5) 6)} |
| Internal resistance of analog source | R_{ASRC} SR | – | $t_S/500$ – 0.25 | k Ω | t_S in [ns] ^{2) 6)} |
| ADC input capacitance | C_{AIN} CC | – | 50 | pF | 6) |

Notes see next page.

Clock Calculation Table

| Clock Prescaler Ratio | ADCL1, 0 | | t_{ADC} | t_S | t_{ADCC} |
|-----------------------|----------|---|--------------------|--------------------|---------------------|
| ÷ 32 | 1 | 1 | $32 \times t_{IN}$ | $64 \times t_{IN}$ | $384 \times t_{IN}$ |
| ÷ 16 | 1 | 0 | $16 \times t_{IN}$ | $32 \times t_{IN}$ | $192 \times t_{IN}$ |
| ÷ 8 | 0 | 1 | $8 \times t_{IN}$ | $16 \times t_{IN}$ | $96 \times t_{IN}$ |
| ÷ 4 | 0 | 0 | $4 \times t_{IN}$ | $8 \times t_{IN}$ | $48 \times t_{IN}$ |

Further timing conditions:

$$t_{ADC} \text{ min} = 500 \text{ ns}$$

$$t_{IN} = 2/f_{OSC} = 2 t_{CLCL}$$

Notes:

- 1) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be X000_H or X3FF_H, respectively.
- 2) During the sample time, the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S . After the end of the sample time t_S , changes of the analog input voltage have no effect on the conversion result.
- 3) This parameter includes the sample time t_S , the time for determining the digital result and the time for the calibration. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.
- 4) T_{UE} is tested at $V_{AREF} = 5.0 \text{ V}$, $V_{AGND} = 0 \text{ V}$, $V_{DD} = 4.9 \text{ V}$. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.
- 5) During the conversion, the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.
- 6) Not 100% tested, but guaranteed by design characterization.

AC Characteristics for C504-L / C504-2R / C504-2E

(Operating Conditions apply)

 (C_L for Port 0, ALE and PSEN outputs = 100 pF; C_L for all other outputs = 80 pF)

| Parameter | Symbol | Limit Values | | | | Unit |
|-----------|--------|--------------|------|---|------|------|
| | | 12-MHz clock | | Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 12 \text{ MHz}$ | | |
| | | min. | max. | min. | max. | |

Program Memory Characteristics

| | | | | | | | |
|--|-----------------|----|-----|-----|------------------|-------------------|----|
| ALE pulse width | t_{LHLL} | CC | 127 | – | $2t_{CLCL} - 40$ | – | ns |
| Address setup to ALE | t_{AVLL} | CC | 43 | – | $t_{CLCL} - 40$ | – | ns |
| Address hold after ALE | t_{LLAX} | CC | 30 | – | $t_{CLCL} - 23$ | – | ns |
| ALE low to valid instr in | t_{LLIV} | SR | – | 233 | – | $4t_{CLCL} - 100$ | ns |
| ALE to $\overline{\text{PSEN}}$ | t_{LLPL} | CC | 58 | – | $t_{CLCL} - 25$ | – | ns |
| $\overline{\text{PSEN}}$ pulse width | t_{PLPH} | CC | 215 | – | $3t_{CLCL} - 35$ | – | ns |
| $\overline{\text{PSEN}}$ to valid instr in | t_{PLIV} | SR | – | 150 | – | $3t_{CLCL} - 100$ | ns |
| Input instruction hold after $\overline{\text{PSEN}}$ | t_{PXIX} | SR | 0 | – | 0 | – | ns |
| Input instruction float after $\overline{\text{PSEN}}$ | $t_{PXIZ}^{1)}$ | SR | – | 63 | – | $t_{CLCL} - 20$ | ns |
| Address valid after $\overline{\text{PSEN}}$ | $t_{PXAV}^{1)}$ | CC | 75 | – | $t_{CLCL} - 8$ | – | ns |
| Address to valid instr in | t_{AVIV} | SR | – | 302 | – | $5t_{CLCL} - 115$ | ns |
| Address float to $\overline{\text{PSEN}}$ | t_{AZPL} | CC | 0 | – | 0 | – | ns |

Notes:

- 1) Interfacing the C504 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

AC Characteristics for C504-L / C504-2R / C504-2E (cont'd)

| Parameter | Symbol | Limit Values | | | | Unit |
|-----------|--------|--------------|------|---|------|------|
| | | 12-MHz clock | | Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 12 \text{ MHz}$ | | |
| | | min. | max. | min. | max. | |

External Data Memory Characteristics

| | | | | | | |
|---|----------------|-----|-----|-------------------|-------------------|----|
| \overline{RD} pulse width | t_{RLRH} CC | 400 | – | $6t_{CLCL} - 100$ | – | ns |
| \overline{WR} pulse width | t_{WLWH} CC | 400 | – | $6t_{CLCL} - 100$ | – | ns |
| Address hold after ALE | t_{LLAX2} CC | 114 | – | $2t_{CLCL} - 53$ | – | ns |
| \overline{RD} to valid data in | t_{RLDV} SR | – | 252 | – | $5t_{CLCL} - 165$ | ns |
| Data hold after \overline{RD} | t_{RHDX} SR | 0 | – | 0 | – | ns |
| Data float after \overline{RD} | t_{RHDZ} SR | – | 97 | – | $2t_{CLCL} - 70$ | ns |
| ALE to valid data in | t_{LLDV} SR | – | 517 | – | $8t_{CLCL} - 150$ | ns |
| Address to valid data in | t_{AVDV} SR | – | 585 | – | $9t_{CLCL} - 165$ | ns |
| ALE to \overline{WR} or \overline{RD} | t_{LLWL} CC | 200 | 300 | $3t_{CLCL} - 50$ | $3t_{CLCL} + 50$ | ns |
| Address valid to \overline{WR} or \overline{RD} | t_{AVWL} CC | 203 | – | $4t_{CLCL} - 130$ | – | ns |
| \overline{WR} or \overline{RD} high to ALE high | t_{WHLH} CC | 43 | 123 | $t_{CLCL} - 40$ | $t_{CLCL} + 40$ | ns |
| Data valid to \overline{WR} transition | t_{QVWX} CC | 33 | – | $t_{CLCL} - 50$ | – | ns |
| Data setup before \overline{WR} | t_{QVWH} CC | 433 | – | $7t_{CLCL} - 150$ | – | ns |
| Data hold after \overline{WR} | t_{WHQX} CC | 33 | – | $t_{CLCL} - 50$ | – | ns |
| Address float after \overline{RD} | t_{RLAZ} CC | – | 0 | – | 0 | ns |

External Clock Drive Characteristics

| Parameter | Symbol | Limit Values | | Unit |
|-------------------|---------------|---|-----------------------|------|
| | | Variable Clock Freq. = 3.5 MHz to 12 MHz | | |
| | | min. | max. | |
| Oscillator period | t_{CLCL} SR | 83.3 | 294 | ns |
| High time | t_{CHCX} SR | 20 | $t_{CLCL} - t_{CLCX}$ | ns |
| Low time | t_{CLCX} SR | 20 | $t_{CLCL} - t_{CHCX}$ | ns |
| Rise time | t_{CLCH} SR | – | 20 | ns |
| Fall time | t_{CHCL} SR | – | 20 | ns |

AC Characteristics for C504-L24 / C504-2R24 / C504-2E24

(Operating Conditions apply)

 (C_L for Port 0, ALE and PSEN outputs = 100 pF; C_L for all other outputs = 80 pF)

| Parameter | Symbol | Limit Values | | | | Unit |
|-----------|--------|--------------|------|---|------|------|
| | | 24-MHz clock | | Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 24 \text{ MHz}$ | | |
| | | min. | max. | min. | max. | |

Program Memory Characteristics

| | | | | | | | |
|--|-----------------|----|----|-----|------------------|------------------|----|
| ALE pulse width | t_{LHLL} | CC | 43 | – | $2t_{CLCL} - 40$ | – | ns |
| Address setup to ALE | t_{AVLL} | CC | 17 | – | $t_{CLCL} - 25$ | – | ns |
| Address hold after ALE | t_{LLAX} | CC | 17 | – | $t_{CLCL} - 25$ | – | ns |
| ALE low to valid instr in | t_{LLIV} | SR | – | 80 | – | $4t_{CLCL} - 87$ | ns |
| ALE to $\overline{\text{PSEN}}$ | t_{LLPL} | CC | 22 | – | $t_{CLCL} - 20$ | – | ns |
| $\overline{\text{PSEN}}$ pulse width | t_{PLPH} | CC | 95 | – | $3t_{CLCL} - 30$ | – | ns |
| $\overline{\text{PSEN}}$ to valid instr in | t_{PLIV} | SR | – | 60 | – | $3t_{CLCL} - 65$ | ns |
| Input instruction hold after $\overline{\text{PSEN}}$ | t_{PXIX} | SR | 0 | – | 0 | – | ns |
| Input instruction float after $\overline{\text{PSEN}}$ | $t_{PXIZ}^{1)}$ | SR | – | 32 | – | $t_{CLCL} - 10$ | ns |
| Address valid after $\overline{\text{PSEN}}$ | $t_{PXAV}^{1)}$ | CC | 37 | – | $t_{CLCL} - 5$ | – | ns |
| Address to valid instr in | t_{AVIV} | SR | – | 148 | – | $5t_{CLCL} - 60$ | ns |
| Address float to $\overline{\text{PSEN}}$ | t_{AZPL} | CC | 0 | – | 0 | – | ns |

Notes:

- 1) Interfacing the C504 to devices with float times up to 37 ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

AC Characteristics for C504-L24 / C504-2R24 / C504-2E24 (cont'd)

| Parameter | Symbol | Limit Values | | | | Unit |
|-----------|--------|--------------|------|---|------|------|
| | | 24-MHz clock | | Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 24 \text{ MHz}$ | | |
| | | min. | max. | min. | max. | |

External Data Memory Characteristics

| | | | | | | | |
|---|-------------|----|-----|-----|-------------------|-------------------|----|
| \overline{RD} pulse width | t_{RLRH} | CC | 180 | – | $6t_{CLCL} - 70$ | – | ns |
| \overline{WR} pulse width | t_{WLWH} | CC | 180 | – | $6t_{CLCL} - 70$ | – | ns |
| Address hold after ALE | t_{LLAX2} | CC | 56 | – | $2t_{CLCL} - 27$ | – | ns |
| \overline{RD} to valid data in | t_{RLDV} | SR | – | 118 | – | $5t_{CLCL} - 90$ | ns |
| Data hold after \overline{RD} | t_{RHDX} | SR | 0 | – | 0 | – | ns |
| Data float after \overline{RD} | t_{RHDZ} | SR | – | 63 | – | $2t_{CLCL} - 20$ | ns |
| ALE to valid data in | t_{LLDV} | SR | – | 200 | – | $8t_{CLCL} - 133$ | ns |
| Address to valid data in | t_{AVDV} | SR | – | 220 | – | $9t_{CLCL} - 155$ | ns |
| ALE to \overline{WR} or \overline{RD} | t_{LLWL} | CC | 75 | 175 | $3t_{CLCL} - 50$ | $3t_{CLCL} + 50$ | ns |
| Address valid to \overline{WR} | t_{AVWL} | CC | 67 | – | $4t_{CLCL} - 97$ | – | ns |
| \overline{WR} or \overline{RD} high to ALE high | t_{WHLH} | CC | 17 | 67 | $t_{CLCL} - 25$ | $t_{CLCL} + 25$ | ns |
| Data valid to \overline{WR} transition | t_{QVWX} | CC | 5 | – | $t_{CLCL} - 37$ | – | ns |
| Data setup before \overline{WR} | t_{QVWH} | CC | 170 | – | $7t_{CLCL} - 122$ | – | ns |
| Data hold after \overline{WR} | t_{WHQX} | CC | 15 | – | $t_{CLCL} - 27$ | – | ns |
| Address float after \overline{RD} | t_{RLAZ} | CC | – | 0 | – | 0 | ns |

External Clock Drive

| Parameter | Symbol | | Limit Values | | Unit |
|-------------------|------------|----|---|-----------------------|------|
| | | | Variable Clock Freq. = 3.5 MHz to 24 MHz | | |
| | | | min. | max. | |
| Oscillator period | t_{CLCL} | SR | 41.7 | 294 | ns |
| High time | t_{CHCX} | SR | 12 | $t_{CLCL} - t_{CLCX}$ | ns |
| Low time | t_{CLCX} | SR | 12 | $t_{CLCL} - t_{CHCX}$ | ns |
| Rise time | t_{CLCH} | SR | – | 12 | ns |
| Fall time | t_{CHCL} | SR | – | 12 | ns |

AC Characteristics for C504-L40 / C504-2R40 / C504-2E40

 (Operating Conditions apply)¹⁾

 (C_L for Port 0, ALE and PSEN outputs = 100 pF; C_L for all other outputs = 80 pF)

| Parameter | Symbol | Limit Values | | | | Unit |
|-----------|--------|--------------|------|---|------|------|
| | | 40-MHz clock | | Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 40 \text{ MHz}$ | | |
| | | min. | max. | min. | max. | |

Program Memory Characteristics

| | | | | | | | |
|--|--------------------------|----|----|----|------------------|------------------|----|
| ALE pulse width | t_{LHLL} | CC | 35 | – | $2t_{CLCL} - 15$ | – | ns |
| Address setup to ALE | t_{AVLL} | CC | 10 | – | $t_{CLCL} - 15$ | – | ns |
| Address hold after ALE | t_{LLAX} | CC | 10 | – | $t_{CLCL} - 15$ | – | ns |
| ALE low to valid instr in | t_{LLIV} | SR | – | 55 | – | $4t_{CLCL} - 45$ | ns |
| ALE to $\overline{\text{PSEN}}$ | t_{LLPL} | CC | 10 | – | $t_{CLCL} - 15$ | – | ns |
| $\overline{\text{PSEN}}$ pulse width | t_{PLPH} | CC | 60 | – | $3t_{CLCL} - 15$ | – | ns |
| $\overline{\text{PSEN}}$ to valid instr in | t_{PLIV} | SR | – | 25 | – | $3t_{CLCL} - 50$ | ns |
| Input instruction hold after $\overline{\text{PSEN}}$ | t_{PXIX} | SR | 0 | – | 0 | – | ns |
| Input instruction float after $\overline{\text{PSEN}}$ | t_{PXIZ} ²⁾ | SR | – | 20 | – | $t_{CLCL} - 5$ | ns |
| Address valid after $\overline{\text{PSEN}}$ | t_{PXAV} ²⁾ | CC | 20 | – | $t_{CLCL} - 5$ | – | ns |
| Address to valid instr in | t_{AVIV} | SR | – | 65 | – | $5t_{CLCL} - 60$ | ns |
| Address float to $\overline{\text{PSEN}}$ | t_{AZPL} | CC | –5 | – | –5 | – | ns |

Notes:

- 1) SAK-C504 is not specified for 40 MHz operation.
- 2) Interfacing the C504 to devices with float times up to 25 ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

AC Characteristics for C504-L40 / C504-2R40 / C504-2E40 (cont'd)

| Parameter | Symbol | Limit Values | | | | Unit |
|-----------|--------|--------------|------|---|------|------|
| | | 40-MHz clock | | Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 40 \text{ MHz}$ | | |
| | | min. | max. | min. | max. | |

External Data Memory Characteristics

| | | | | | | | |
|---|-------------|----|-----|-----|------------------|------------------|----|
| \overline{RD} pulse width | t_{RLRH} | CC | 120 | – | $6t_{CLCL} - 30$ | – | ns |
| \overline{WR} pulse width | t_{WLWH} | CC | 120 | – | $6t_{CLCL} - 30$ | – | ns |
| Address hold after ALE | t_{LLAX2} | CC | 35 | – | $2t_{CLCL} - 15$ | – | ns |
| \overline{RD} to valid data in | t_{RLDV} | SR | – | 75 | – | $5t_{CLCL} - 50$ | ns |
| Data hold after \overline{RD} | t_{RHDX} | SR | 0 | | 0 | – | ns |
| Data float after \overline{RD} | t_{RHDZ} | SR | – | 38 | – | $2t_{CLCL} - 12$ | ns |
| ALE to valid data in | t_{LLDV} | SR | – | 150 | – | $8t_{CLCL} - 50$ | ns |
| Address to valid data in | t_{AVDV} | SR | – | 150 | – | $9t_{CLCL} - 75$ | ns |
| ALE to \overline{WR} or \overline{RD} | t_{LLWL} | CC | 60 | 90 | $3t_{CLCL} - 15$ | $3t_{CLCL} + 15$ | ns |
| Address valid to \overline{WR} | t_{AVWL} | CC | 70 | – | $4t_{CLCL} - 30$ | – | ns |
| \overline{WR} or \overline{RD} high to ALE high | t_{WHLH} | CC | 10 | 40 | $t_{CLCL} - 15$ | $t_{CLCL} + 15$ | ns |
| Data valid to \overline{WR} transition | t_{QVWX} | CC | 5 | – | $t_{CLCL} - 20$ | – | ns |
| Data setup before \overline{WR} | t_{QVWH} | CC | 125 | – | $7t_{CLCL} - 50$ | – | ns |
| Data hold after \overline{WR} | t_{WHQX} | CC | 5 | – | $t_{CLCL} - 20$ | – | ns |
| Address float after \overline{RD} | t_{RLAZ} | CC | – | 0 | – | 0 | ns |

External Clock Drive

| Parameter | Symbol | Limit Values | | | | Unit |
|-------------------|------------|---|----|------|-----------------------|------|
| | | Variable Clock Freq. = 3.5 MHz to 40 MHz | | | | |
| | | min. | | max. | | |
| Oscillator period | t_{CLCL} | SR | 25 | | 294 | ns |
| High time | t_{CHCX} | SR | 10 | | $t_{CLCL} - t_{CLCX}$ | ns |
| Low time | t_{CLCX} | SR | 10 | | $t_{CLCL} - t_{CHCX}$ | ns |
| Rise time | t_{CLCH} | SR | – | | 10 | ns |
| Fall time | t_{CHCL} | SR | – | | 10 | ns |

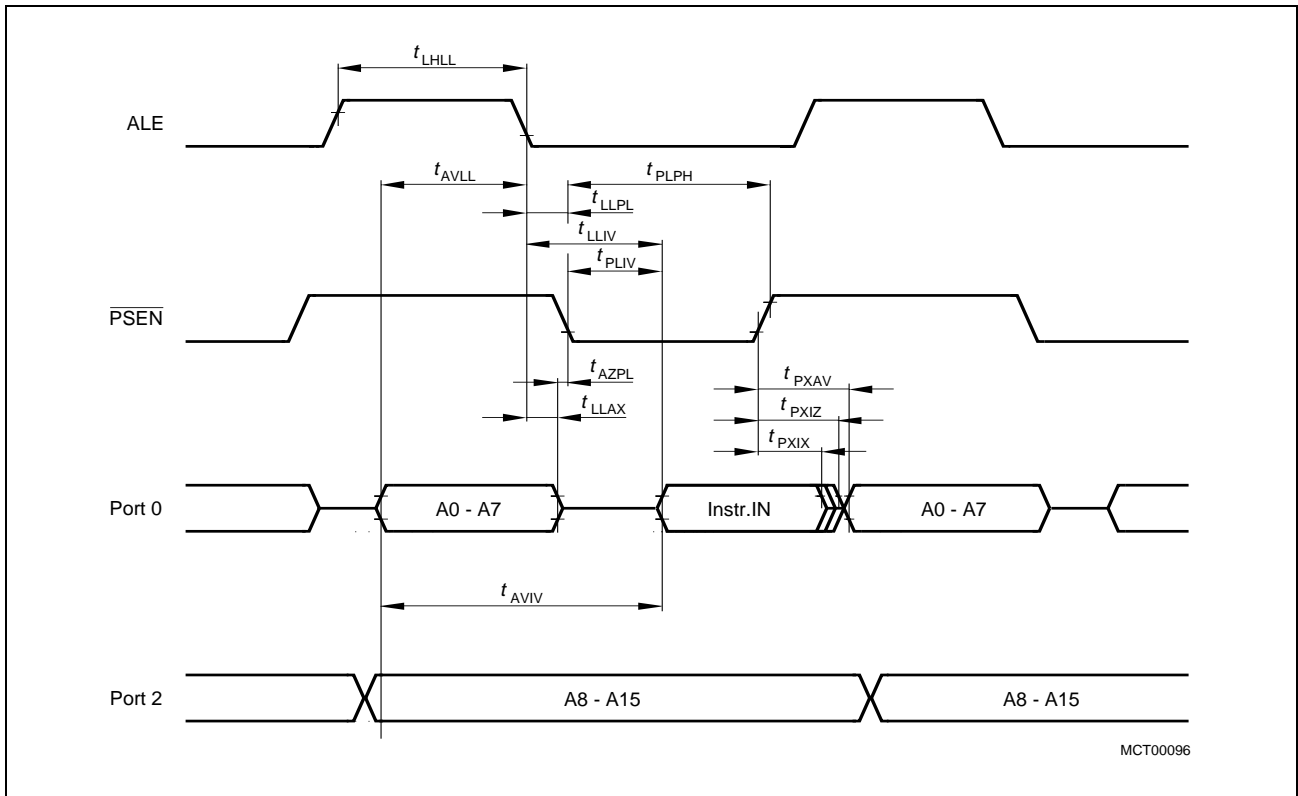


Figure 24 Program Memory Read Cycle

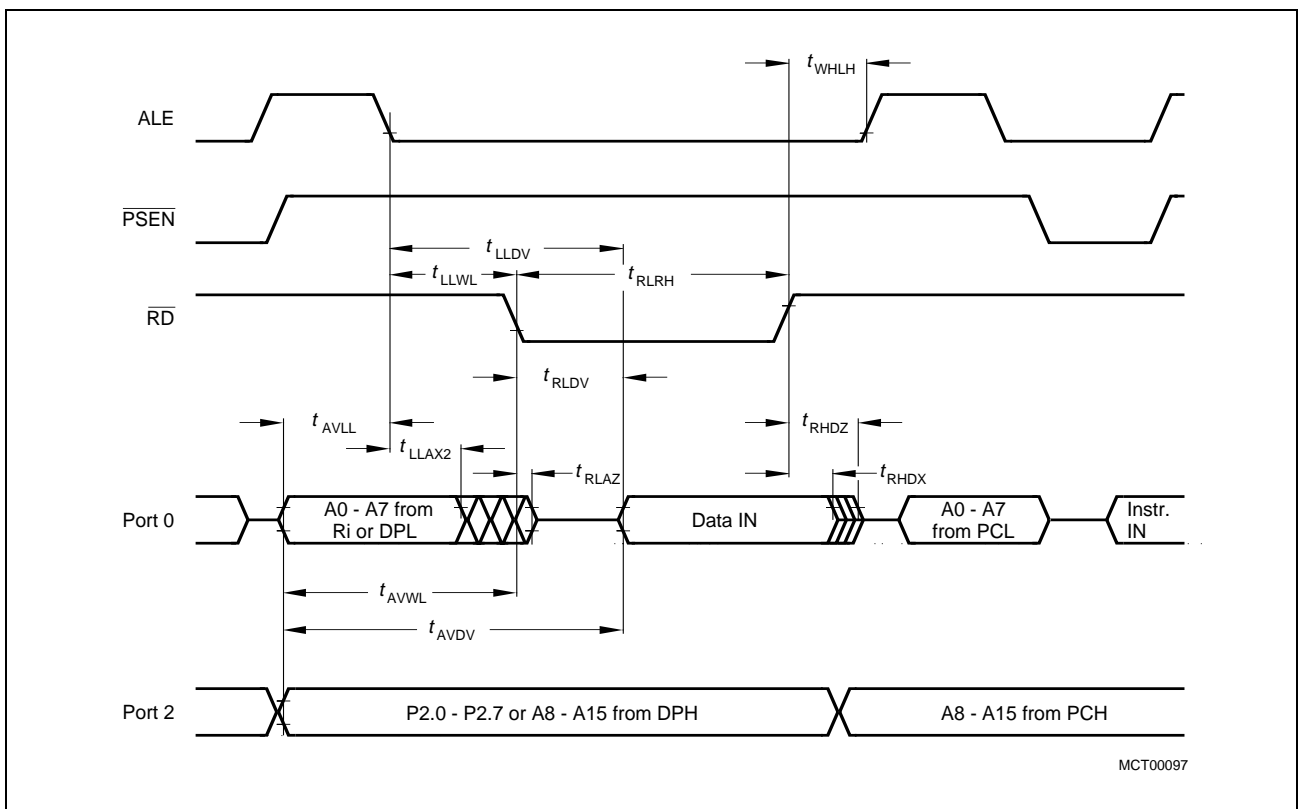


Figure 25 Data Memory Read Cycle

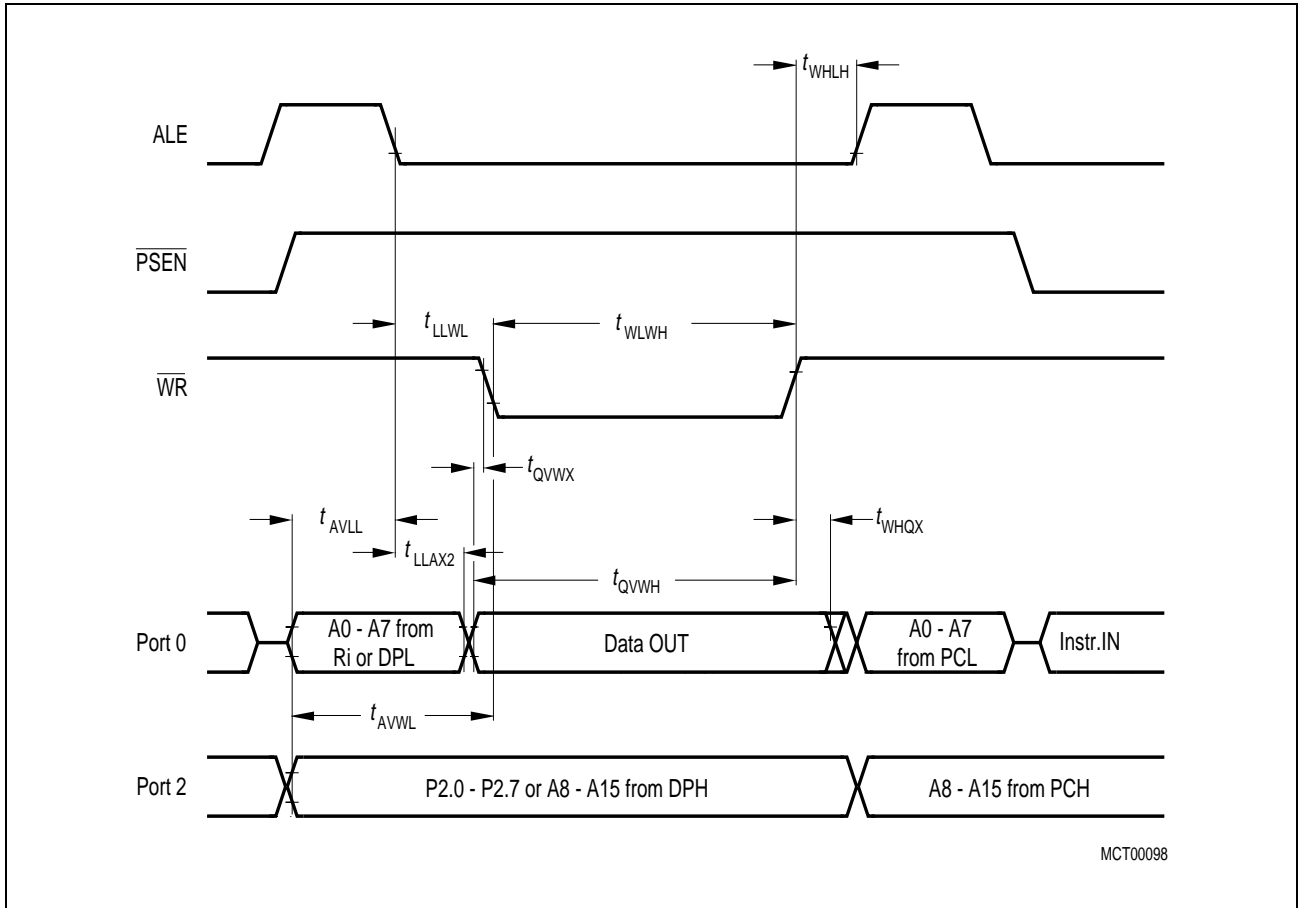


Figure 26 Data Memory Write Cycle

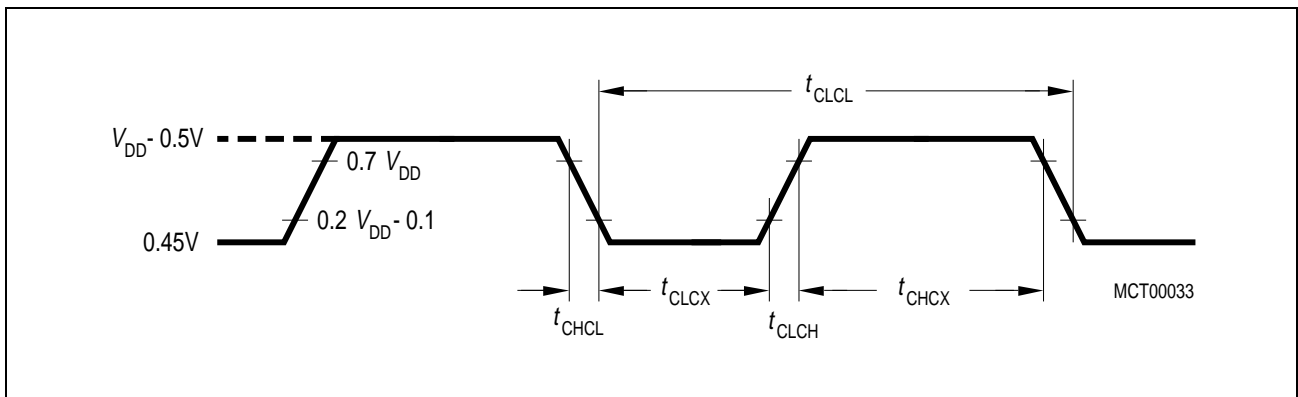


Figure 27 External Clock Cycle

AC Characteristics of Programming Mode
 $(V_{DD} = 5\text{ V} \pm 10\%; V_{PP} = 11.5\text{ V} \pm 5\%; T_A = 25\text{ }^\circ\text{C} \pm 10\text{ }^\circ\text{C})$

| Parameter | Symbol | Limit Values | | Unit |
|---|------------|--------------|-------|---------------|
| | | min. | max. | |
| PALE pulse width | t_{PAW} | 35 | – | ns |
| PMSEL setup to PALE rising edge | t_{PMS} | 10 | – | ns |
| Address setup to PALE, $\overline{\text{PROG}}$, or $\overline{\text{PRD}}$ falling edge | t_{PAS} | 10 | – | ns |
| Address hold after PALE, $\overline{\text{PROG}}$, or $\overline{\text{PRD}}$ falling edge | t_{PAH} | 10 | – | ns |
| Address, data setup to $\overline{\text{PROG}}$ or $\overline{\text{PRD}}$ | t_{PCS} | 100 | – | ns |
| Address, data hold after $\overline{\text{PROG}}$ or $\overline{\text{PRD}}$ | t_{PCH} | 0 | – | ns |
| PMSEL setup to $\overline{\text{PROG}}$ or $\overline{\text{PRD}}$ | t_{PMS} | 10 | – | ns |
| PMSEL hold after $\overline{\text{PROG}}$ or $\overline{\text{PRD}}$ | t_{PMH} | 10 | – | ns |
| $\overline{\text{PROG}}$ pulse width | t_{PWW} | 100 | – | μs |
| $\overline{\text{PRD}}$ pulse width | t_{PRW} | 100 | – | ns |
| Address to valid data out | t_{PAD} | – | 75 | ns |
| $\overline{\text{PRD}}$ to valid data out | t_{PRD} | – | 20 | ns |
| Data hold after $\overline{\text{PRD}}$ | t_{PDH} | 0 | – | ns |
| Data float after $\overline{\text{PRD}}$ | t_{PDF} | – | 20 | ns |
| $\overline{\text{PROG}}$ high between two consecutive $\overline{\text{PROG}}$ low pulses | t_{PWH1} | 1 | – | μs |
| $\overline{\text{PRD}}$ high between two consecutive $\overline{\text{PRD}}$ low pulses | t_{PWH2} | 100 | – | ns |
| XTAL clock period | t_{CLKP} | 83.3 | 285.7 | ns |

Note:

$V_{PP} = 11.5\text{ V} \pm 5\%$ is valid for devices with version byte 2 = 02_H or higher. Devices with version byte 2 = 01_H must be programmed with $V_{PP} = 12\text{ V} \pm 5\%$.

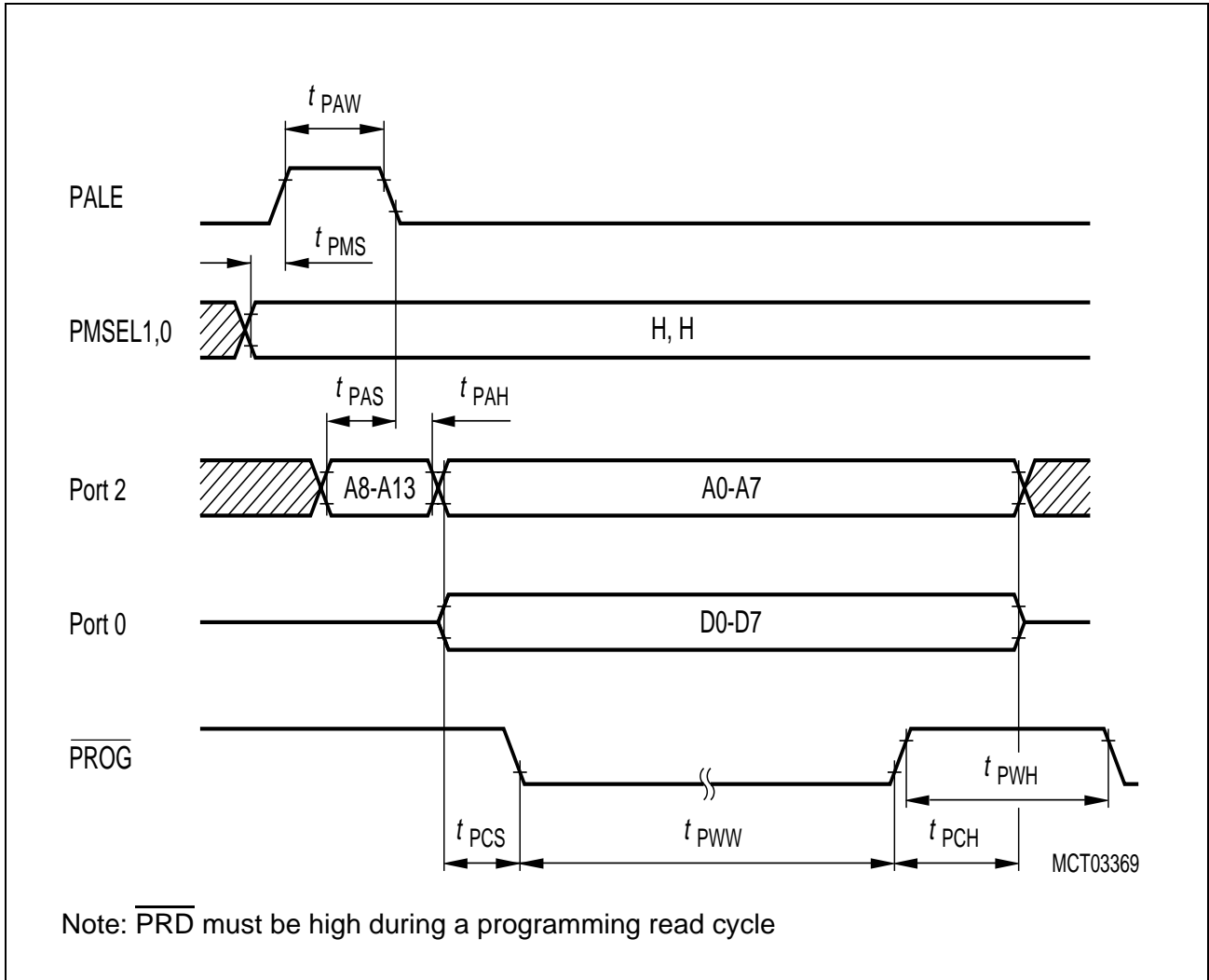


Figure 28 Programming Code Byte - Write Cycle Timing

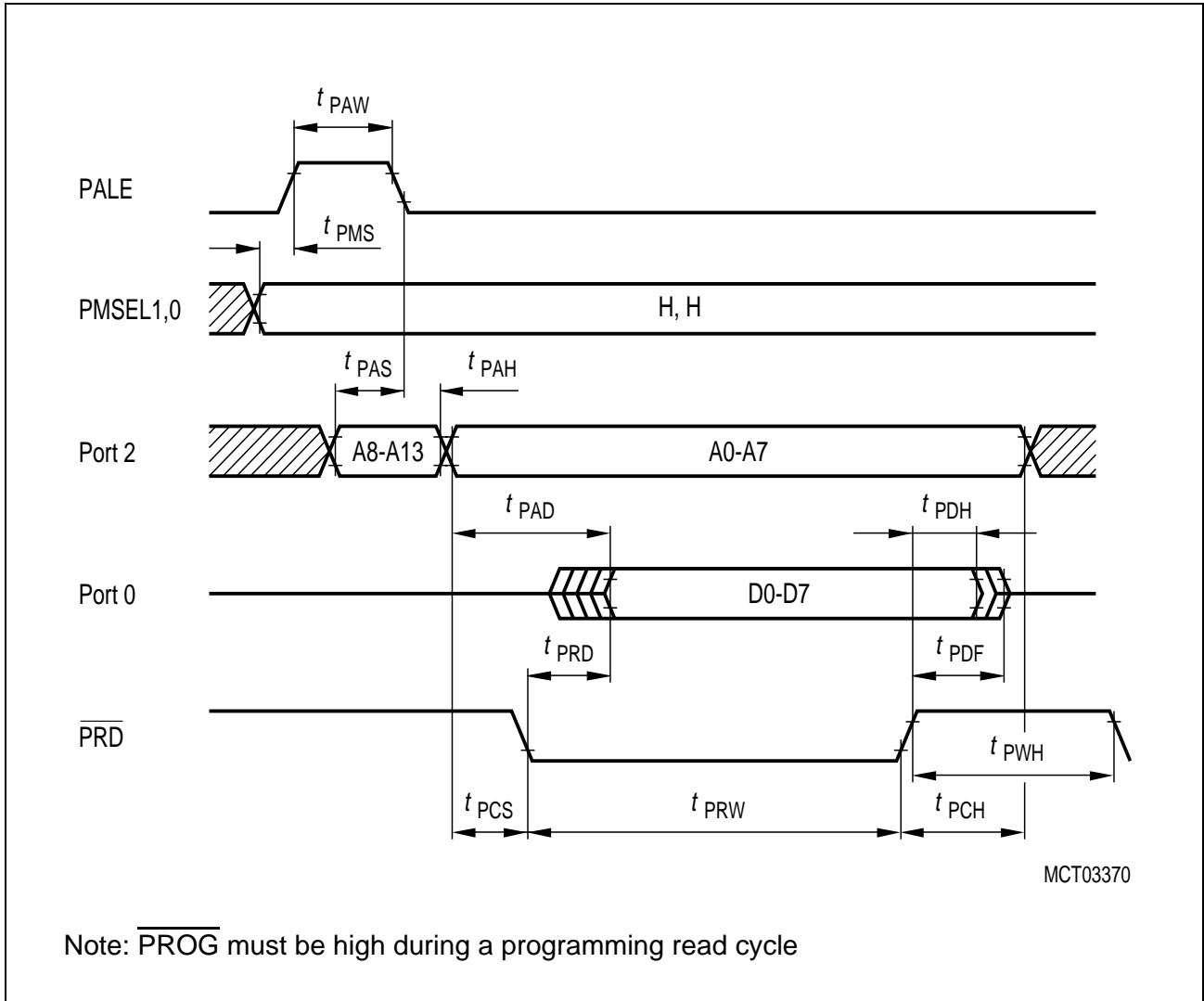


Figure 29 Verify Code Byte - Read Cycle Timing

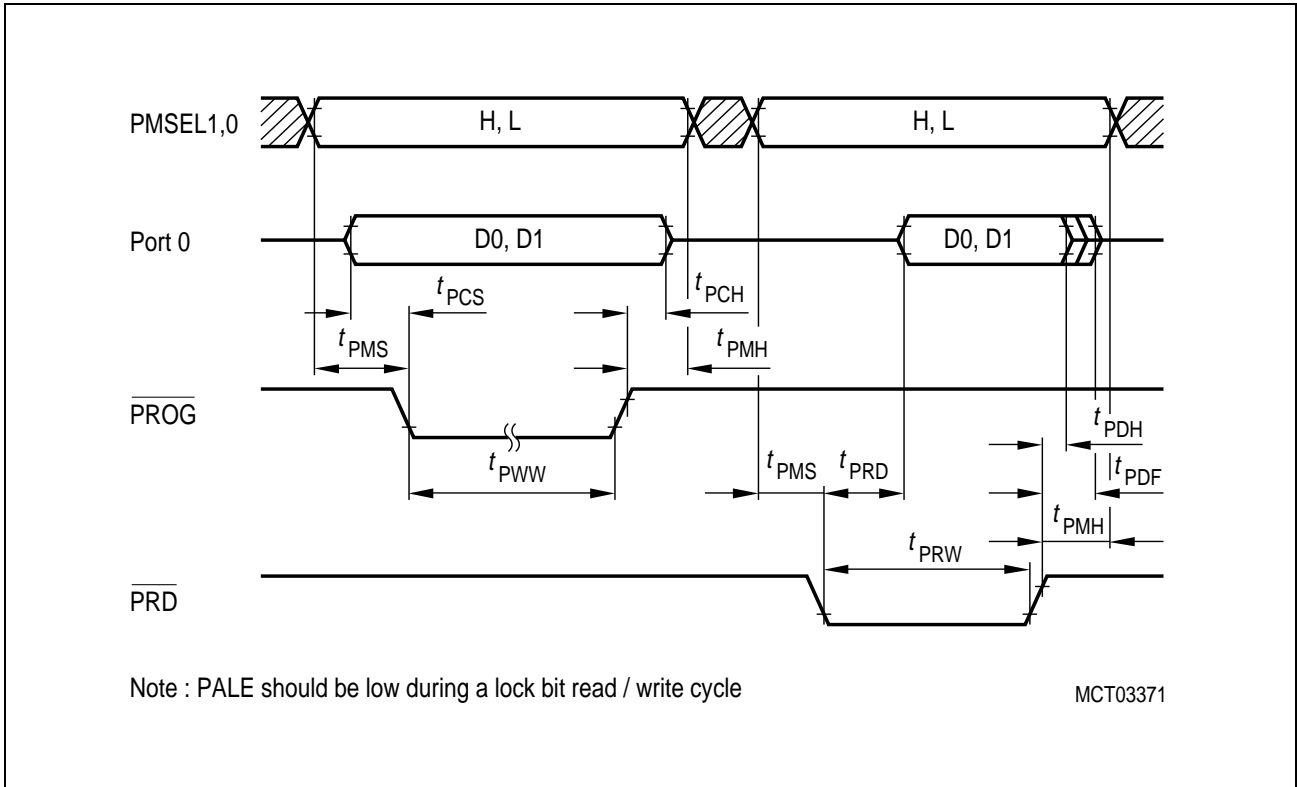


Figure 30 Lock Bit Access Timing

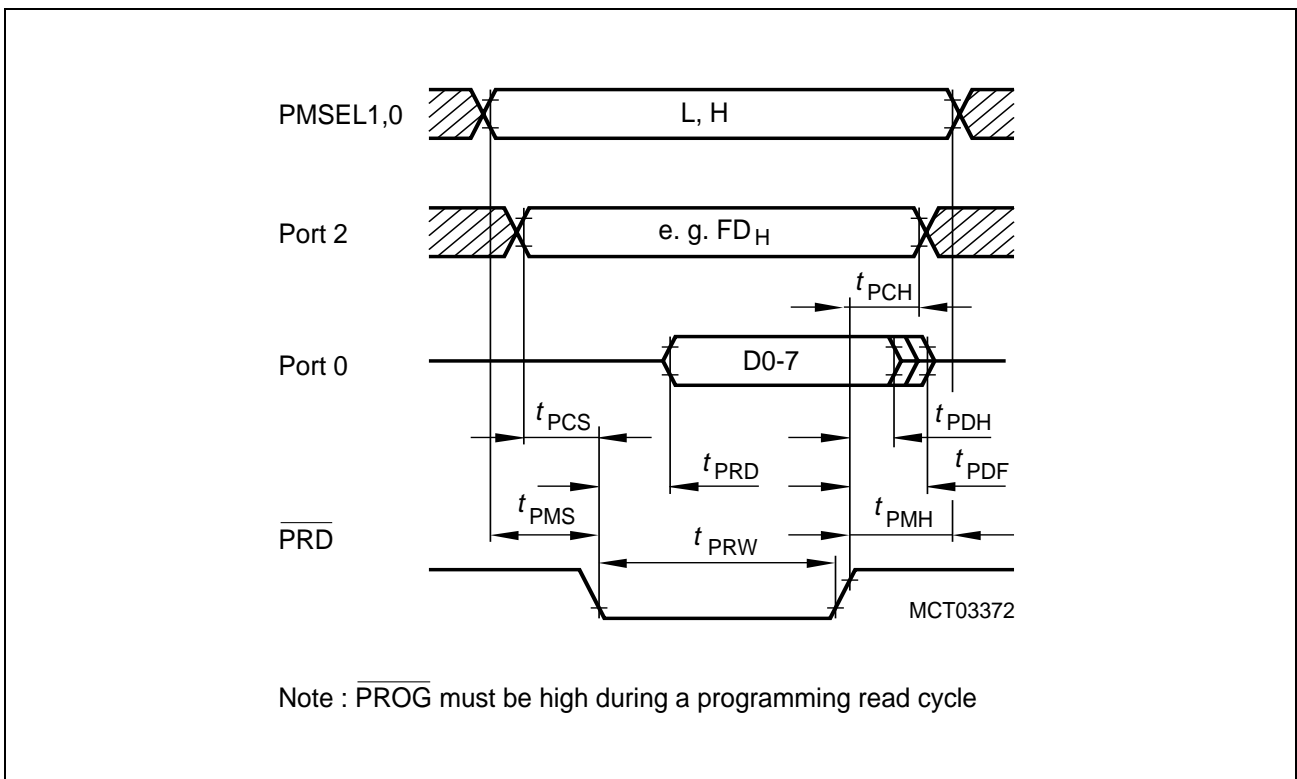


Figure 31 Version Byte Read Timing

ROM/OTP Verification Characteristics for C504-2R / C504-2E
ROM Verification Mode 1 (C504-2R only)

| Parameter | Symbol | Limit Values | | Unit |
|-----------------------|------------|--------------|---------------|------|
| | | min. | max. | |
| Address to valid data | t_{AVQV} | — | $10 t_{CLCL}$ | ns |

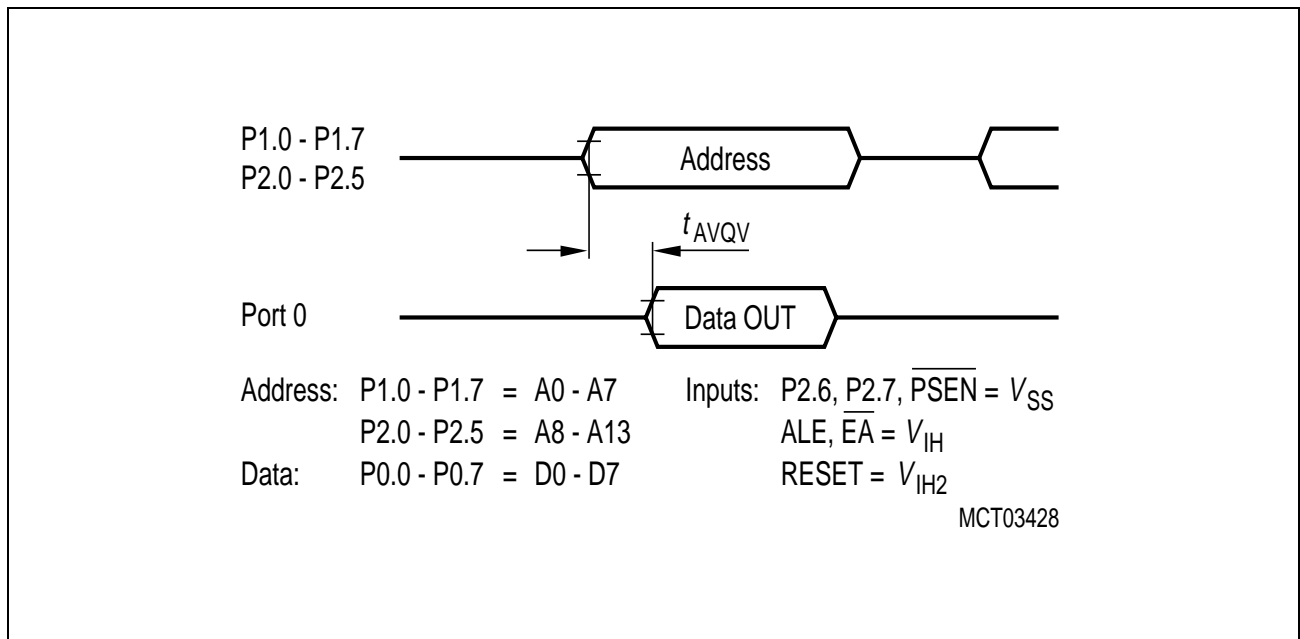


Figure 32 ROM Verification Mode 1

ROM/OTP Verification Mode 2

| Parameter | Symbol | Limit Values | | | Unit |
|-----------------------|--------------|--------------|---------------|--------------|------|
| | | min. | typ | max. | |
| ALE pulse width | t_{AWD} | – | $2 t_{CLCL}$ | – | ns |
| ALE period | t_{ACY} | – | $12 t_{CLCL}$ | – | ns |
| Data valid after ALE | t_{DVA} | – | – | $4 t_{CLCL}$ | ns |
| Data stable after ALE | t_{DSA} | $8 t_{CLCL}$ | – | – | ns |
| P3.5 setup to ALE low | t_{AS} | – | t_{CLCL} | – | ns |
| Oscillator frequency | $1/t_{CLCL}$ | 4 | – | 6 | MHz |

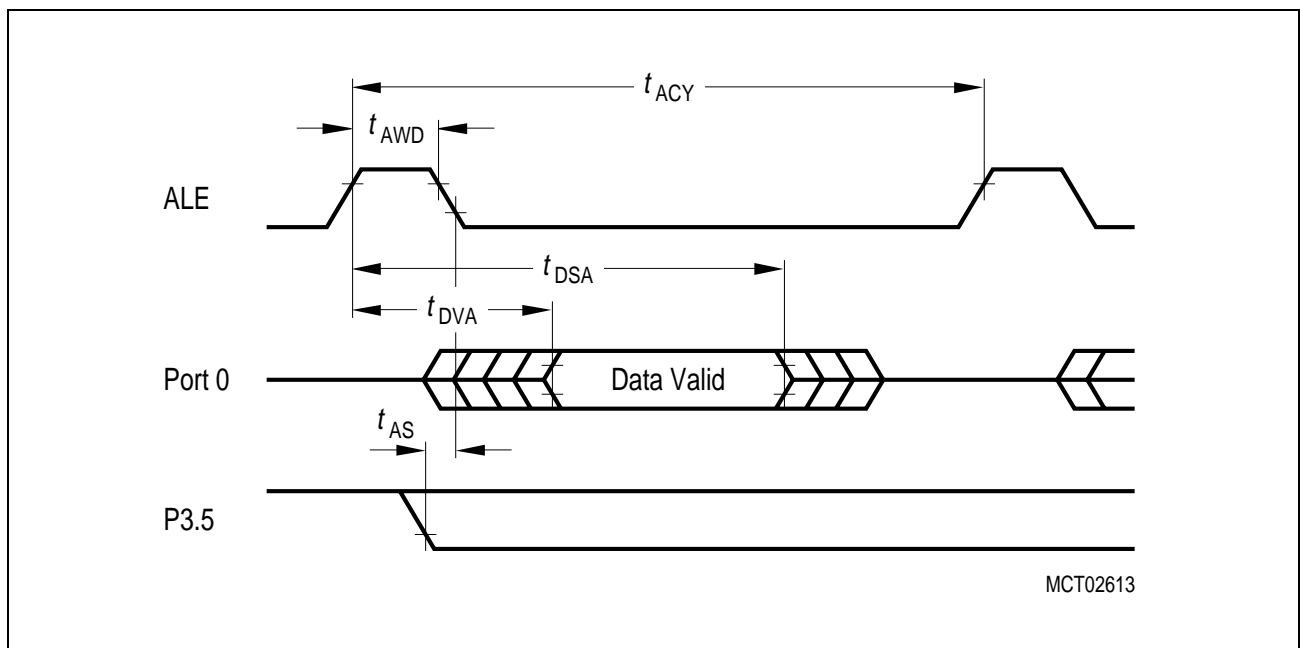


Figure 33 ROM Verification Mode 2

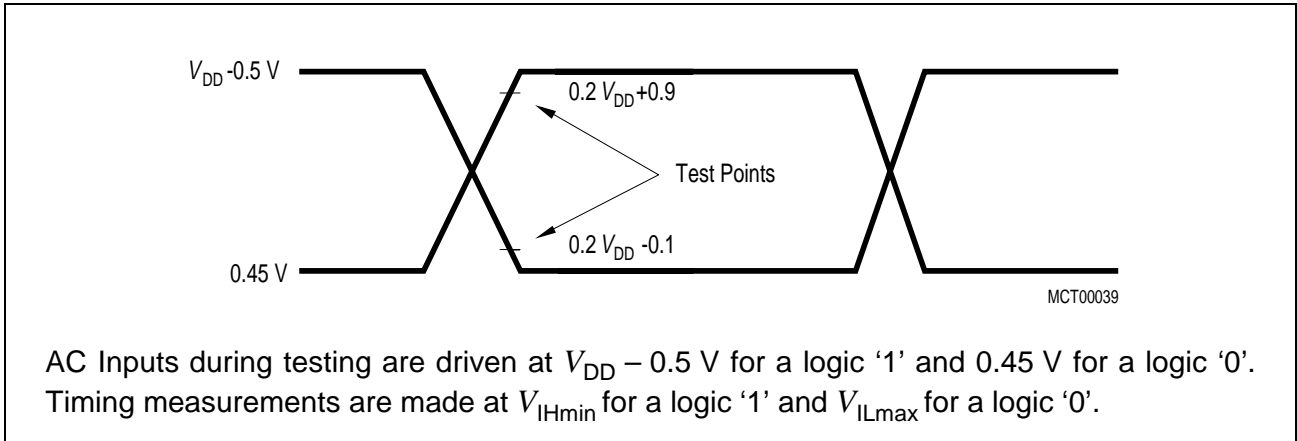


Figure 34 AC Testing: Input, Output Waveforms

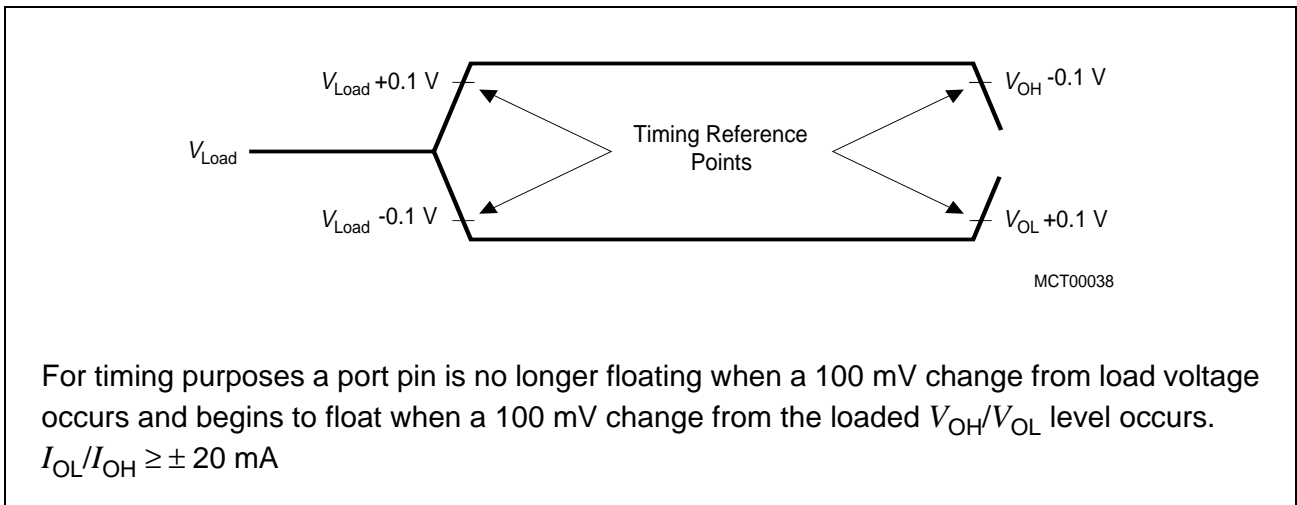


Figure 35 AC Testing: Float Waveforms

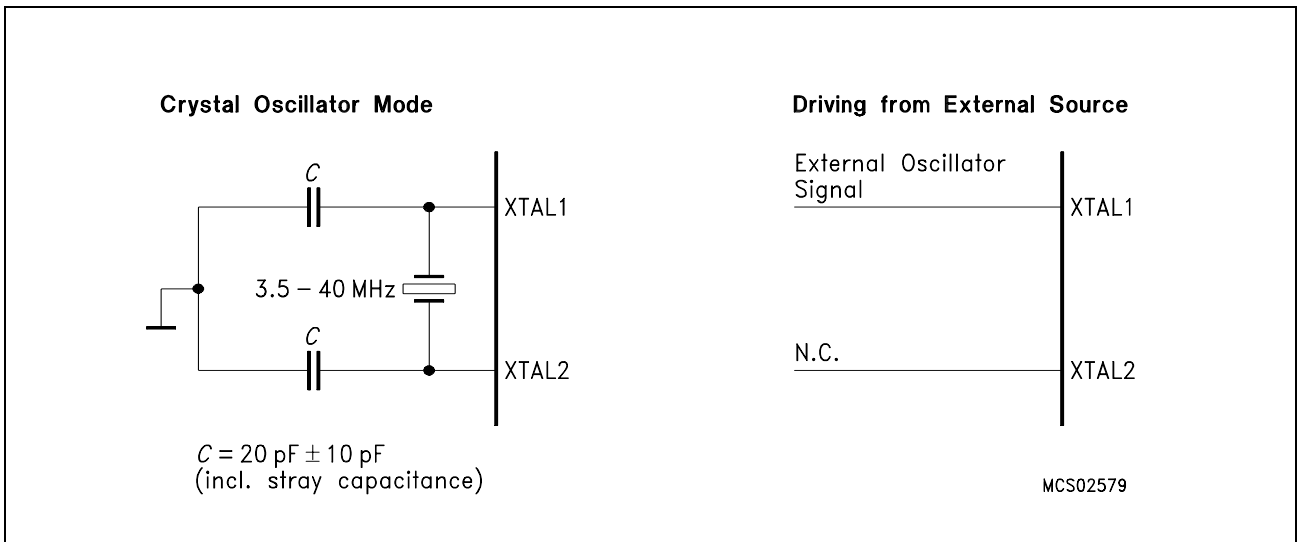
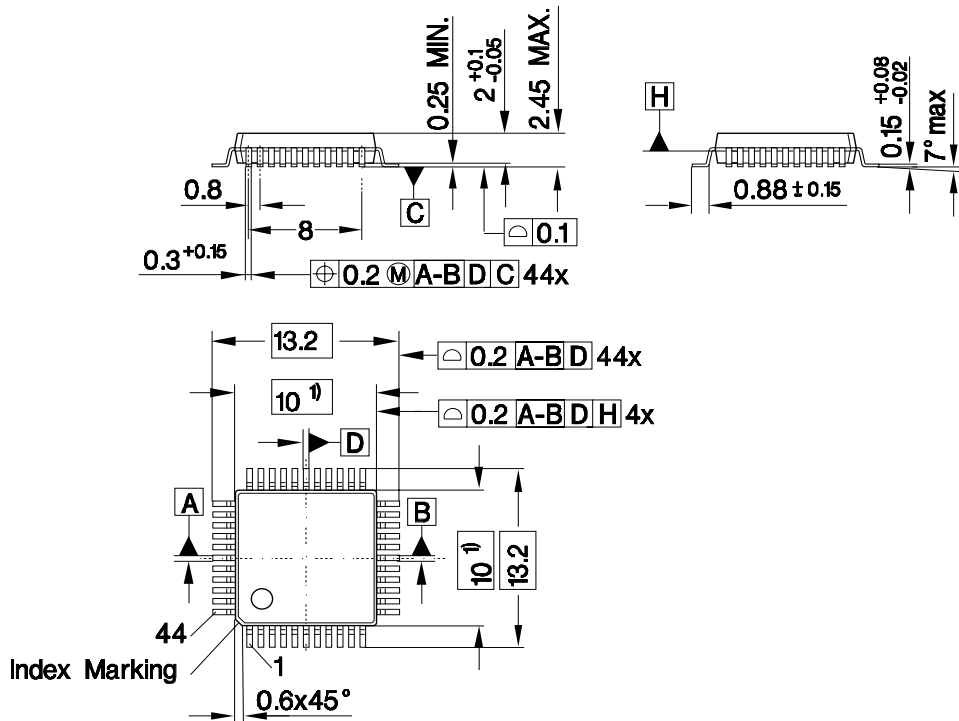


Figure 36 Recommended Oscillator Circuits for Crystal Oscillator

Package Information

P-MQFP-44 (SMD)
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPM05622

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

Infineon goes for Business Excellence

“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.

Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

<http://www.infineon.com>