1. SCOPE

2. WARRANTY

3. FEATURES

- Small Molecular Organic Light Emission Diode.
- Color : 262K and 65k Full colors
- Panel matrix : 128*3*128
- Driver IC : SSD1339
- Excellent Quick response time : 10μs
- Extremely thin thickness for best mechanism design : 1.45 mm
- High contrast : 500:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 8/16-bit 6800-series Parallel Interface, 8/16-bit 8080-series Parallel Interface, Serial Peripheral.
- Wide range of operating temperature : -40 to 70°C

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x (RxGxB) x 128 (H)	dot
2	Dot Size	0.0555 (W) x 0.1855 (H)	mm^2
3	Dot Pitch	0.0685 (W) x 0.2055 (H)	mm^2
4	Aperture Rate	73	%
5	Active Area	26.291 (W) x 26.284 (H)	mm^2
6	Panel Size	33.5 (W) x 33.5 (H)	mm^2
7	Panel Thickness	1.45 ± 0.1	mm
8	Module Size	33.5 (W) x 47.5 (H) x 1.45 (D)	mm^3
9	Diagonal A/A size	1.46	inch
10	Module Weight	3.6 ± 10%	gram

5. MAXIMUM RATING

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})		3.5	V	Ta = 25°C	IC maximum rating
Supply Voltage(Vcc)	8	18	V	Ta = 25°C	IC maximum rating
Operating Temp.	-40	70	°C		
Storage Temp	-40	85	°C		
Humidity		85	%		
Life Time	8,000	-	Hrs	100 cd/m2, 50% checkerboard	Note (1)
Life Time	10,000	-	Hrs	80 cd/m2, 50% checkerboard	Note (2)
Life Time	13,000	-	Hrs	60 cd/m2, 50% checkerboard	Note (3)

Note:

(A) Under Vcc = 16 Volts, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 100cd/m2 :

- Master contrast setting : 0x0D
- Frame rate : 85Hz
- Duty setting : 1/128

(2) Setting of 80cd/m2 :

- Master contrast setting : 0x09
- Frame rate : 85Hz
- Duty setting : 1/128

(3) Setting of 60cd/m2 :

- Master contrast setting : 0x06
- Frame rate : 85Hz
- Duty setting : 1/128

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Driver power supply (for OLED panel)	Ta=-20 °C to +70°C	15.5	16	16.5	V
V_{DD}	Logic operating voltage	Ta=-20 °C to +70°C	2.4	2.7	3.5	V
V_{DDIO}	Logic I/O operating voltage	Ta=-20 °C to +70°C	1.5	1.8	3.5	V
I_{DD}	V_{DD} supply current	V_{DD}=3.0V, V_{CC}=18V, Display ON, Contrast =FF, No panel attached	-	1.3	-	mA
I_{CC}	V_{CC} supply current	V_{DD}=3.0V, V_{CC}=18V, Display ON, Contrast =FF, No panel attached	-	0.4	-	mA
V_{IH}	High logic input level	Iout=100uA, 3.3MHz	0.8* V_{DDIO}	-	V_{DDIO}	V
V_{IL}	Low logic input level	Iout=100uA, 3.3MHz	0	-	0.2* V_{DDIO}	V
V_{OH}	High logic output level	Iout=100uA, 3.3MHz	0.9* V_{DDIO}	-	V_{DDIO}	V
V_{OL}	Low logic output level	Iout=100uA, 3.3MHz	0	-	0.1* V_{DDIO}	V
I_{SEG}	Segment output current setting V_{DD}=2.7V, V_{CC}=11V, I_{REF}=10uA, All one pattern, Display on,	Contrast=FF	-	160	-	uA
		Contrast=AF	-	110	-	uA
		Contrast=5F	-	60	-	uA
		Contrast=00	-	0	-	uA

Note 1: V_{DD}= 2.7V ; V_{CC}= 16V ; Frame rate= 85Hz ; No panel attached.

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		33	35	mA	All pixels on (1)
Standby mode current		2	4	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		528	560	mW	All pixels on (1)
Standby mode power consumption		32	64	mW	Standby mode 10% pixels on (2)
Normal mode Luminance	60	80		cd/m^2	Display Average
Standby mode Luminance		20		cd/m^2	
CIEx(White)	0.27	0.31	0.35		x, y (CIE 1931)
CIEy(White)	0.30	0.34	0.38		
CIEx(Red)	0.61	0.65	0.69		
CIEy(Red)	0.30	0.34	0.38		
CIEx(Green)	0.21	0.25	0.29		
CIEy(Green)	0.52	0.56	0.60		
CIEx(Blue)	0.07	0.11	0.15		
CIEy(Blue)	0.13	0.17	0.21		
Dark Room Contrast	500:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

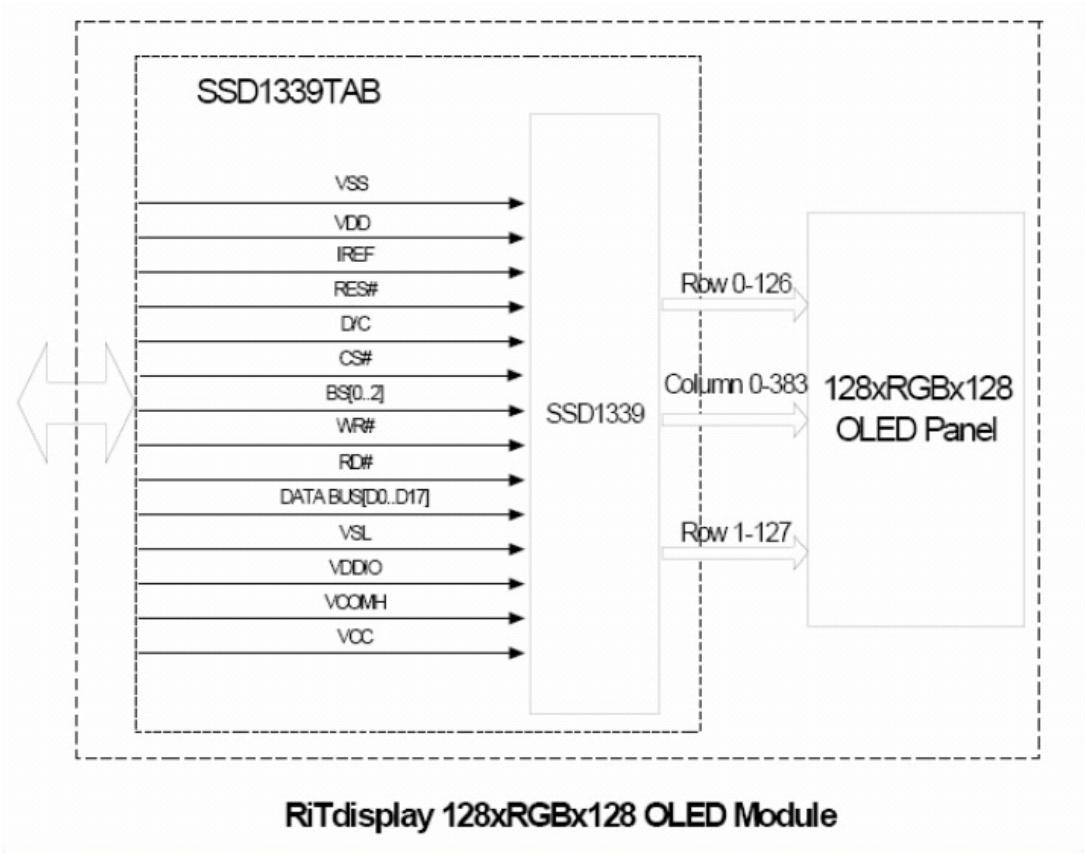
- Driving Voltage : 16V
- Master contrast setting : 0x09
- Frame rate : 85Hz
- Duty setting : 1/128

(2) Standby mode condition :

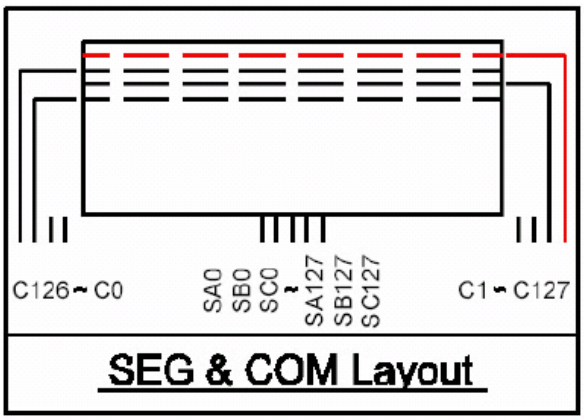
- Driving Voltage : 16V
- Master contrast setting : 0x01
- Frame rate : 85Hz
- Duty setting : 1/128

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

PIN NAME	PIN NO	DESCRIPTION
NC	1	No connection.
VSS	2	Ground.
TEST0	3	No connection.
VDD	4	Digital voltage power supply.
TEST1	5	No connection.
TEST2	6	No connection.
TEST3	7	No connection.
IREF	8	A resistor should be connected between this pin and VSS.
RES#	9	Hardware Reset pin (Low active).
D/C#	10	H: Data, L: Command.
CS#	11	Chip select pin.
BS2	12	Interface select pin.
BS1	13	Interface select pin.
BS0	14	Interface select pin.
R/W#	15	8080: data write enable pin; 6800:Read/Write select pin.
E/RD#	16	8080: data read enable pin; 6800:Read/Write enable pin.
D0	17	16/18 bits data Bus.
D1	18	
D2	19	
D3	20	
D4	21	
D5	22	
D6	23	
D7	24	
D8	25	
D9	26	
D10	27	
D11	28	
D12	29	
D13	30	
D14	31	
D15	32	
D16	33	
D17	34	
VSL	35	This is segment voltage reference pin.
VDDIO	36	I/O voltage power supply.
VCOMH	37	A capacitor should be connected between this pin an VSS.
VCC	38	Analog power supply.
NC	39	No connection.

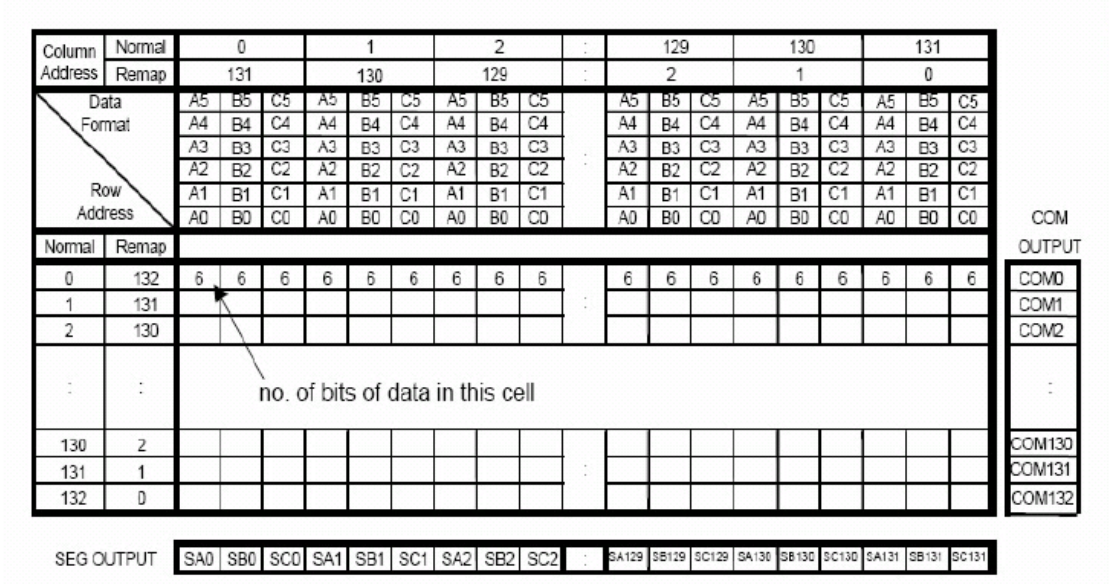
7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132x132x18bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

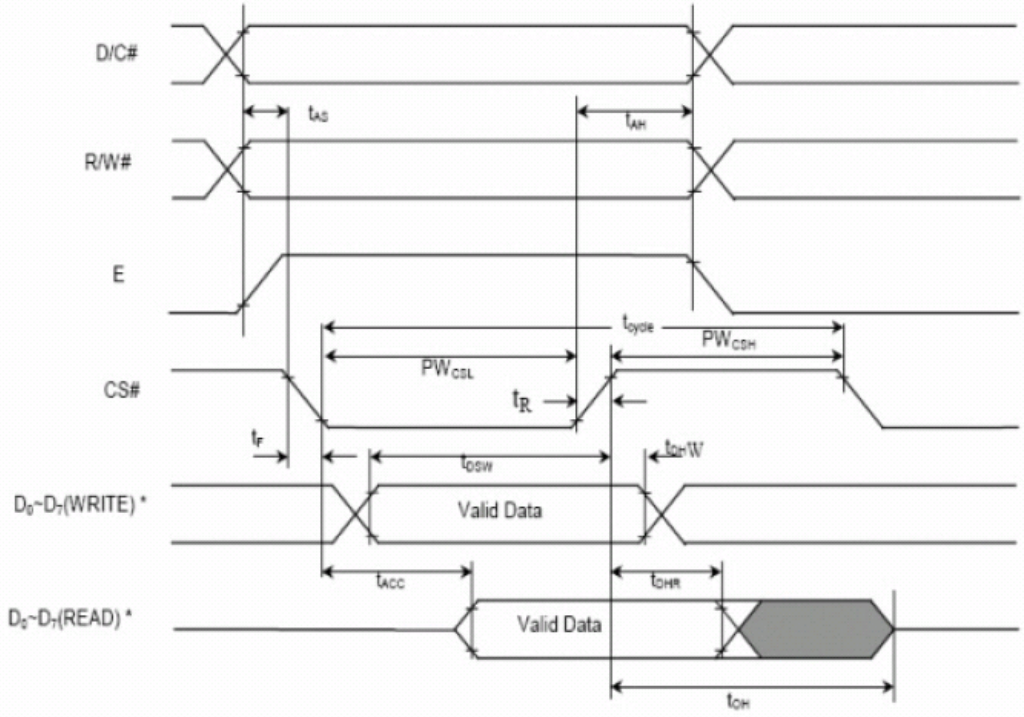
Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown below.



7.5 INTERFACE TIMING CHART

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

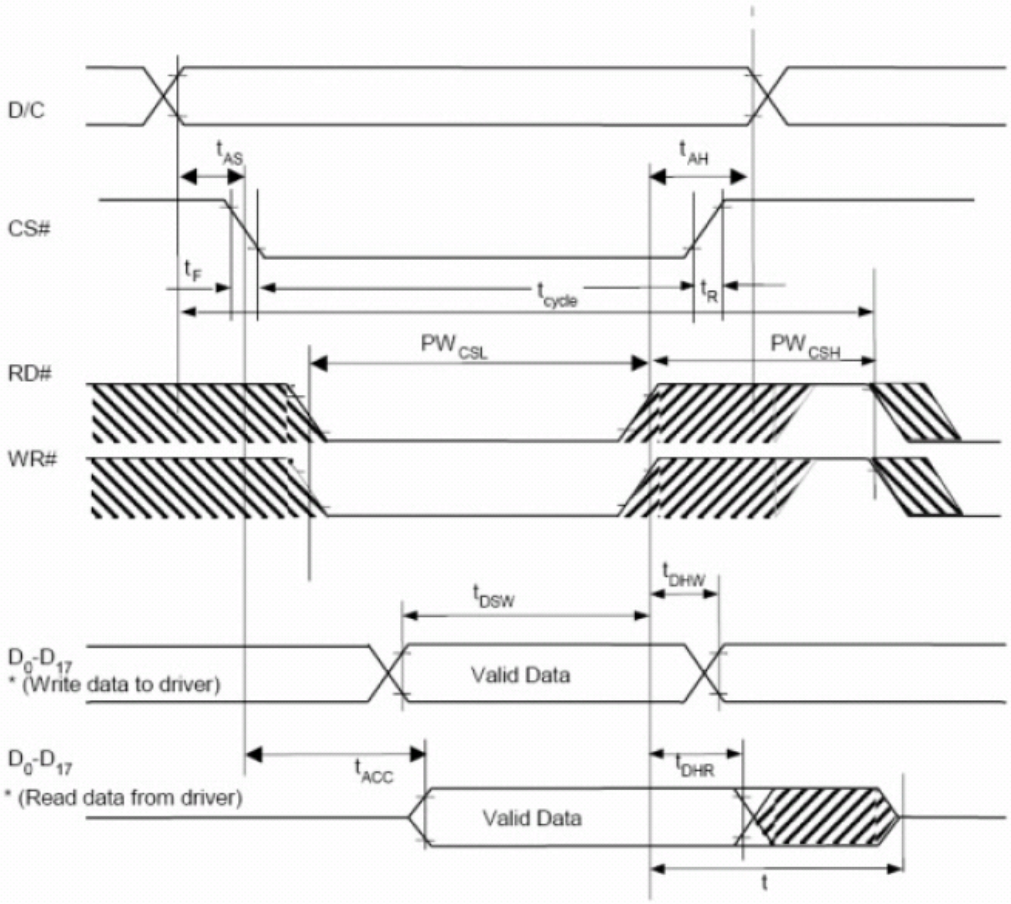
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



6800-series MPU parallel interface characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

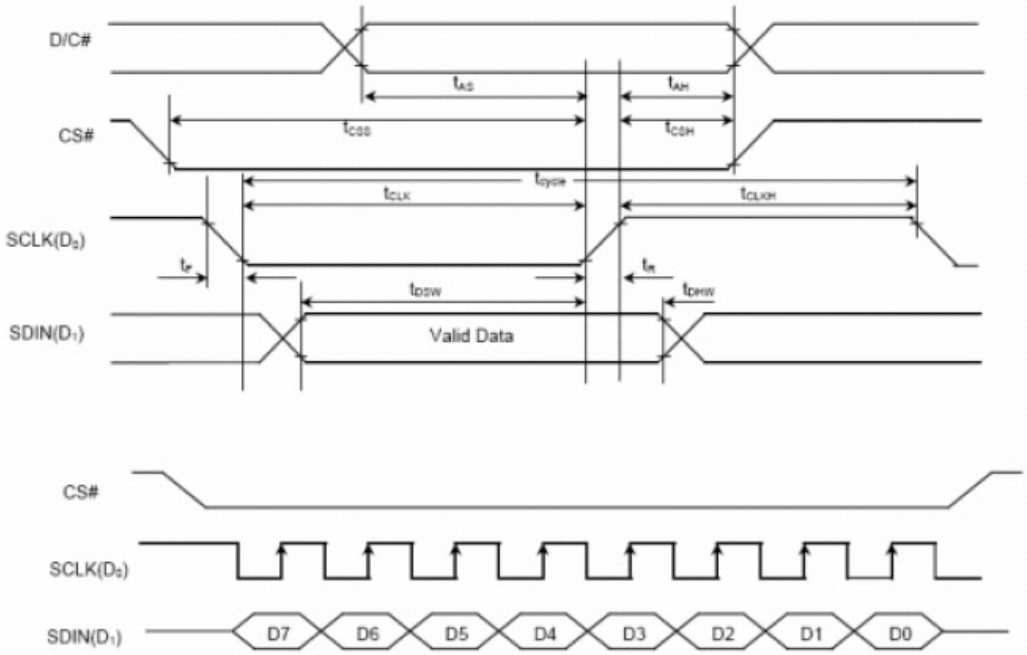
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



8080-series MPU parallel interface characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

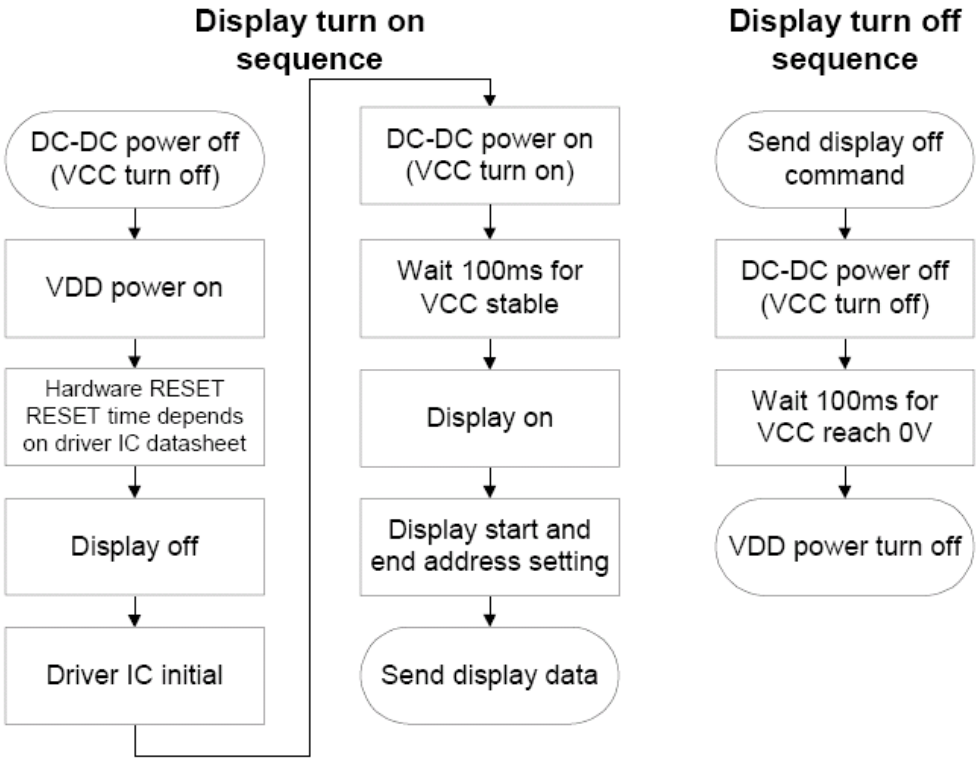
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



Serial interface characteristics

8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE



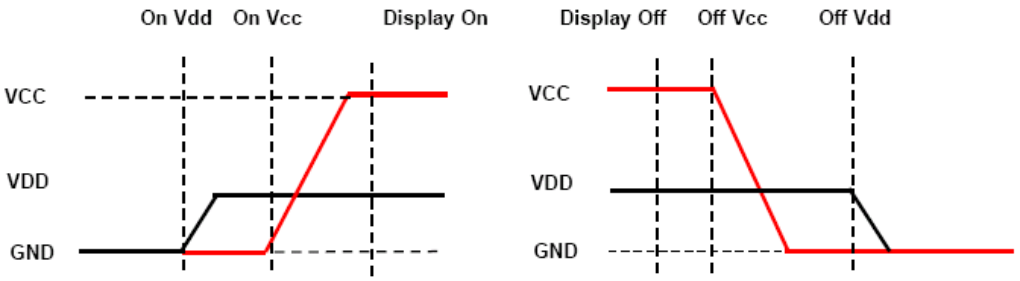
To protect OLED panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources turn on/off.

Power up Sequence:

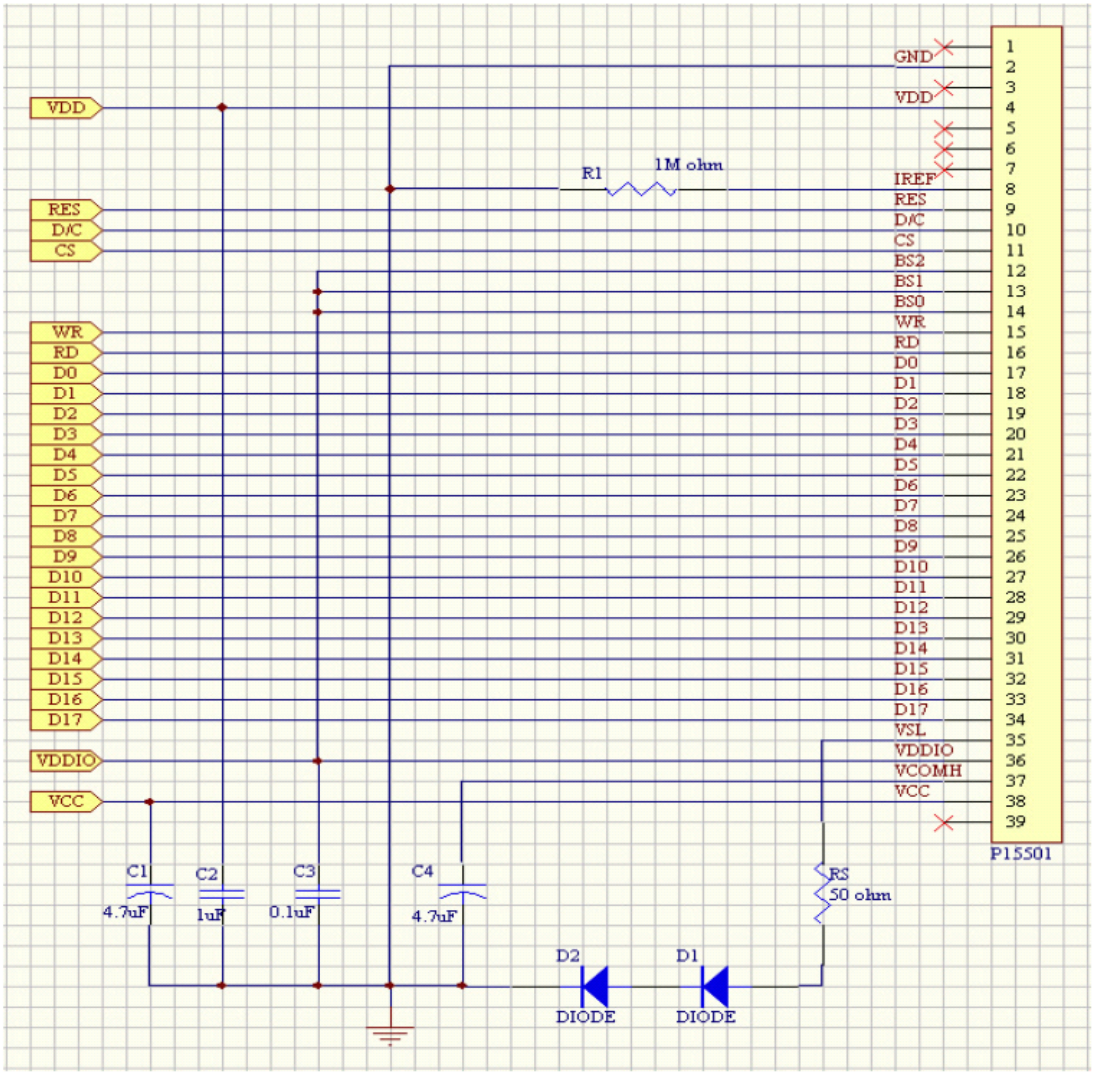
1. **Power up Vdd**
2. **Hardware RESET**
3. **Send display off command**
4. **Power up Vcc**
5. **Delay 100ms (when Vcc is stable)**
6. **Send Display on command**

Power down Sequence:

1. **Send Display off command**
2. **Power down Vcc**
3. **Delay 100ms (When Vcc is reach 0 and panel is completely discharges)**
4. **Power down Vdd**



8.2 APPLICATION CIRCUIT



Component:

C1, C4: 4.7uF/25V or 35V (Tantalum type)

C2: 1uF/25V

C3: 0.1uF/16V

R1: 1M ohm 1%

RS: 50 ohm 1/4W

D1, D2: RB480K(ROHM)

This circuit is for 8080 18bits/16bits interface.

8.3 COMMAND TABLE

Refer to IC Spec.: SSD1339

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 96hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 20 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

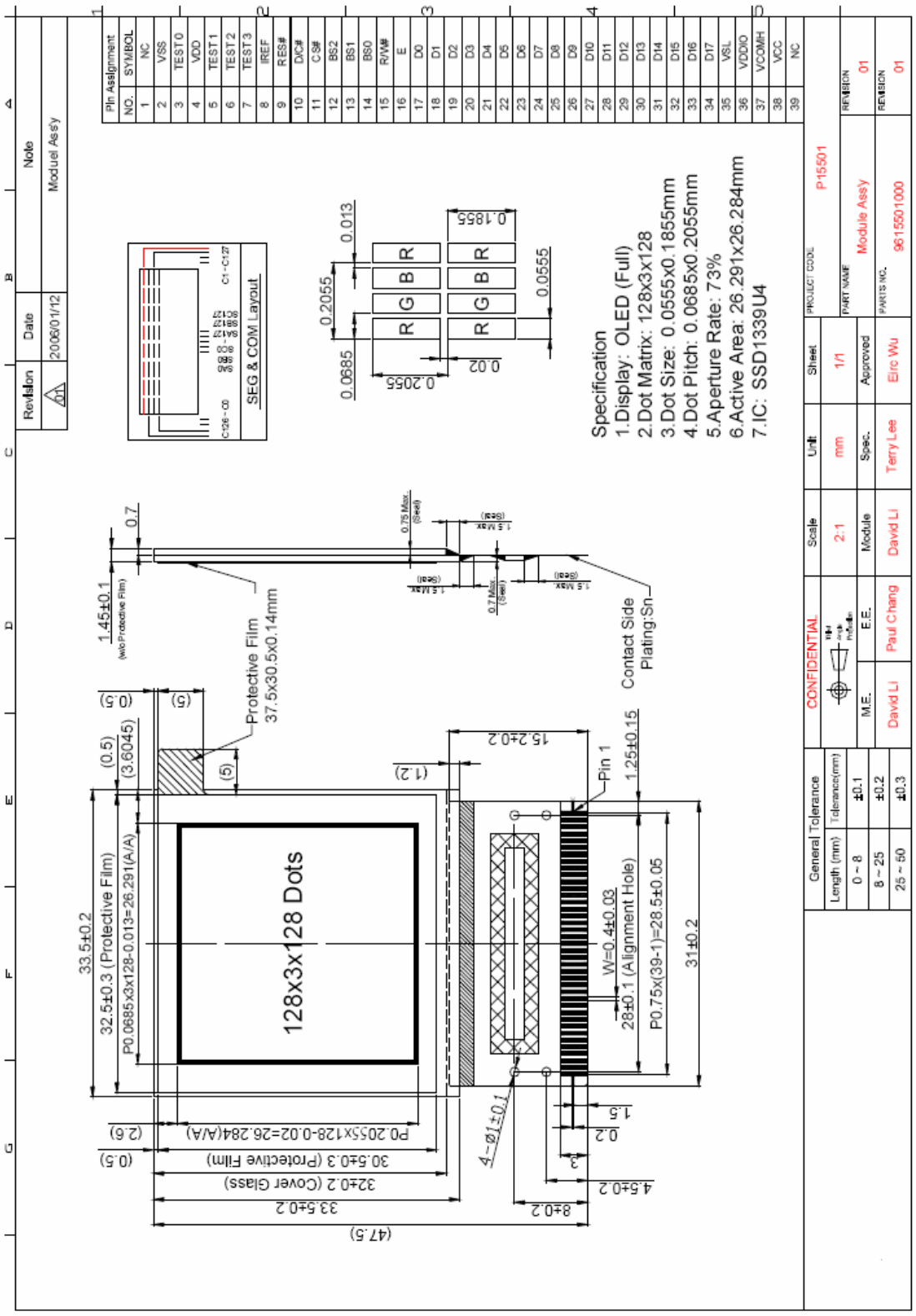
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.

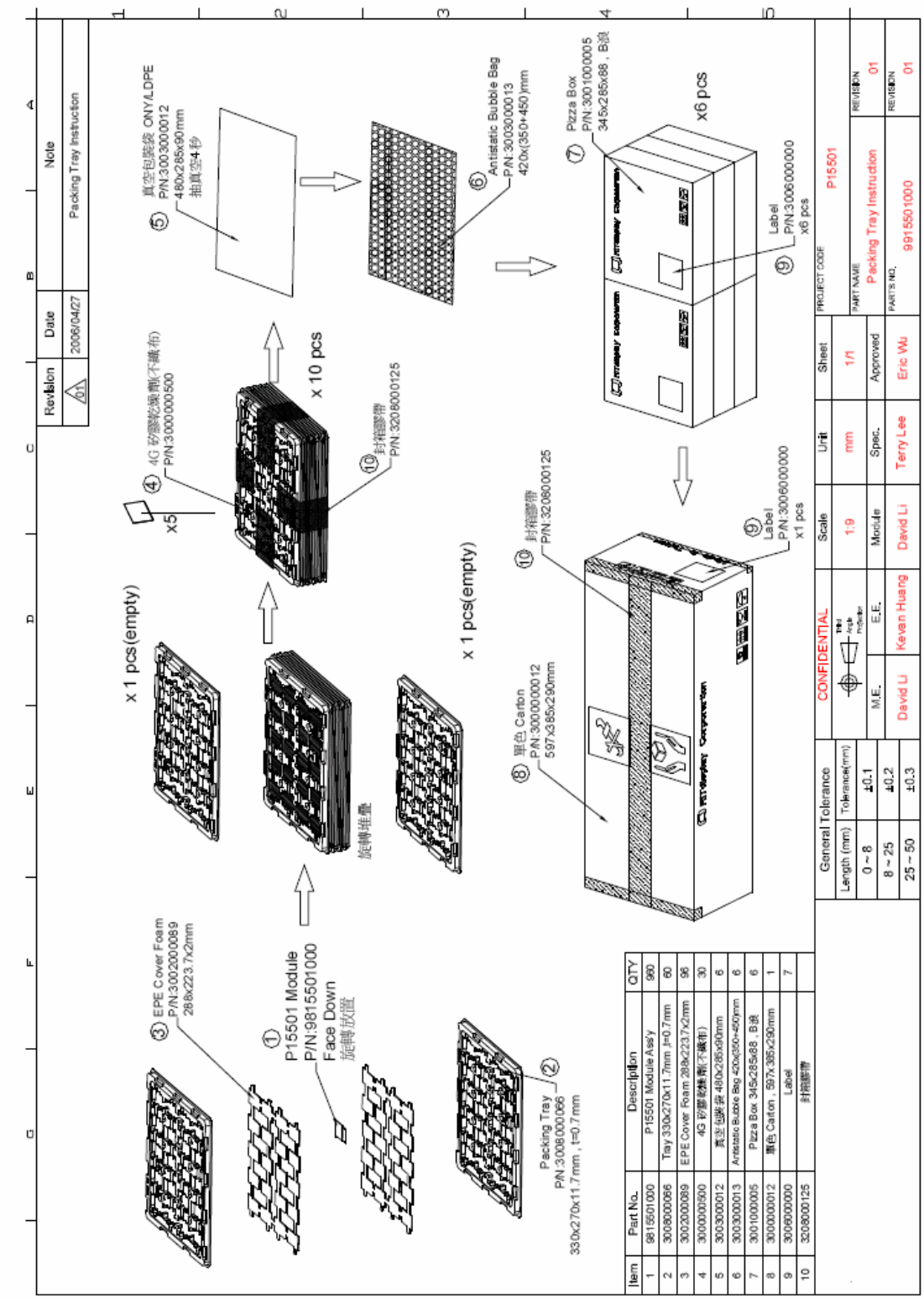
Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

10. EXTERNAL DIMENSION



11. PACKING SPECIFICATION



Item	Part No.	Description	QTY
1	9815501000	P15501 Module Assy	960
2	3008000066	Tray 330x270x11.7mm ,t=0.7mm	60
3	3002000089	EPE Cover Foam 288x223.7X2mm	96
4	3000000500	4G 矽膠乾燥劑(不織布)	30
5	3003000012	真空包裝袋 480x285x90mm	6
6	3003000013	Antistatic Bubble Bag 420x(350+450)mm	6
7	3001000005	Pizza Box 345x285x88 , B級	6
8	3000000012	單色 Carton , 597x 385x290mm	1
9	3006000000	Label	7
10	3208000125	封箱膠帶	

12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

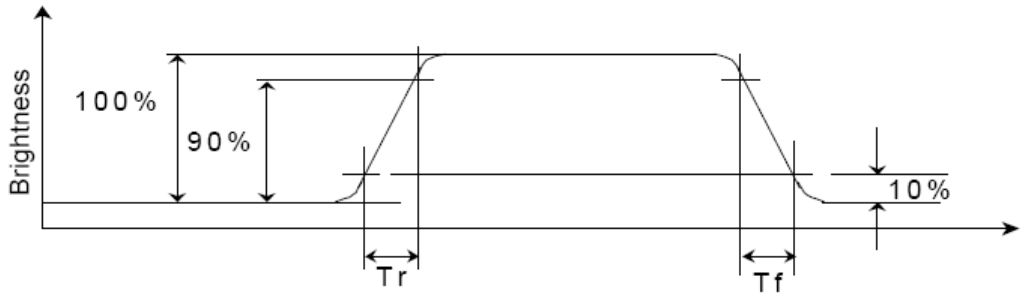
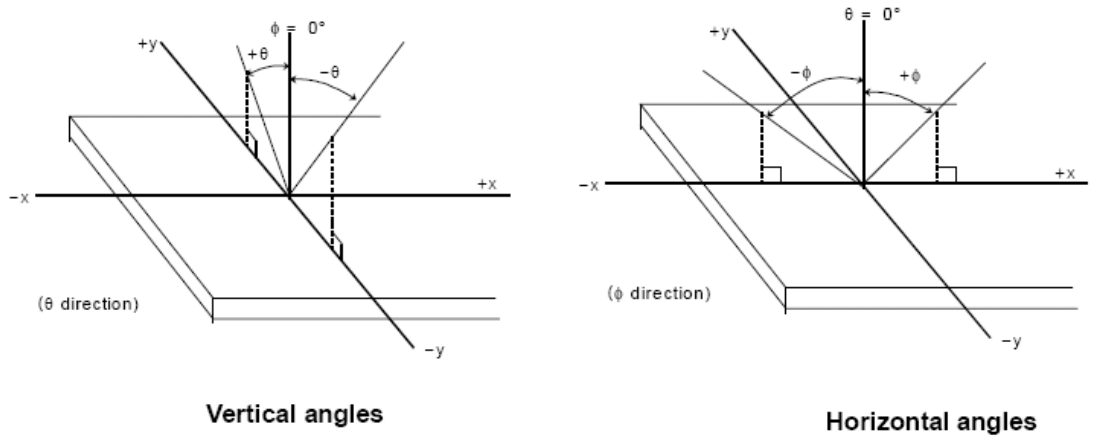


Figure 2: Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.



Vertical angles

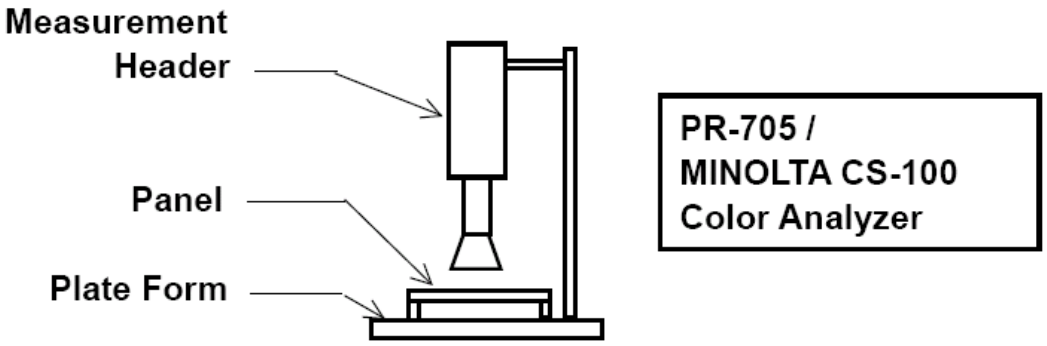
Horizontal angles

Figure 3: Viewing Angle

APPENDIX 2: MEASUREMENT APPARATUS

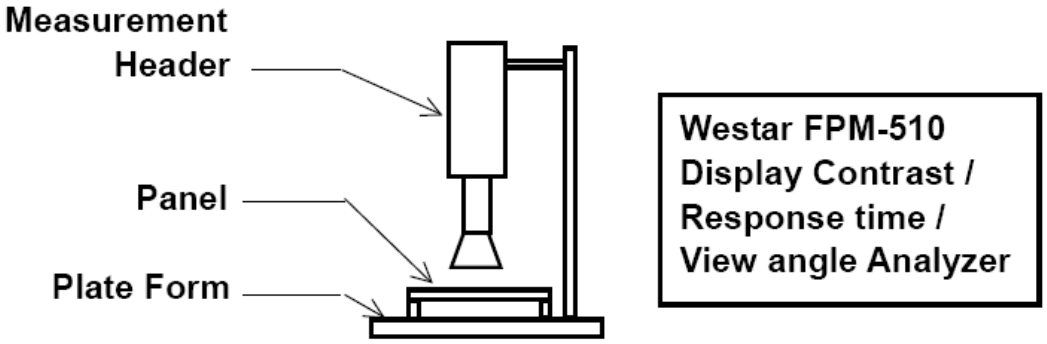
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

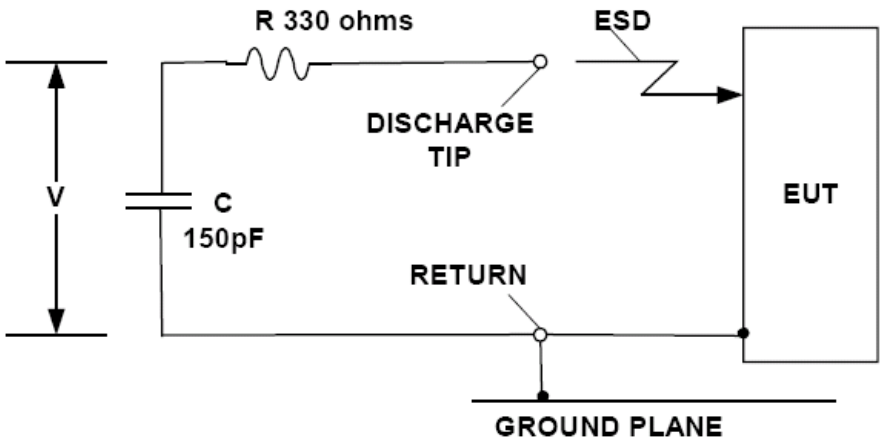


B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.