



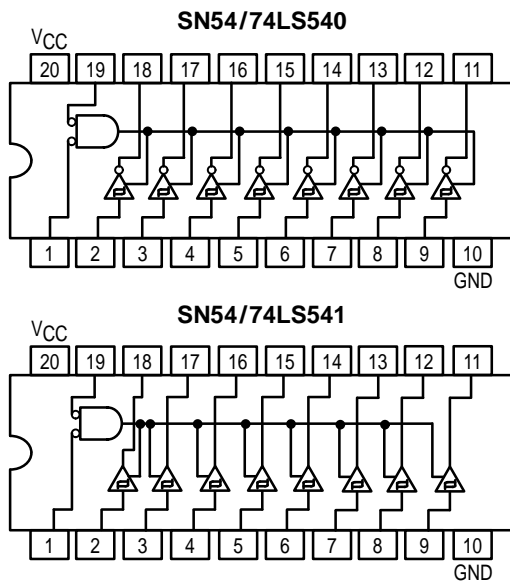
OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

The SN54/74LS540 and SN54/74LS541 are octal buffers and line drivers with the same functions as the LS240 and LS241, but with pinouts on the opposite side of the package.

These device types are designed to be used as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These devices are especially useful as output ports for the microprocessors, allowing ease of layout and greater PC board density.

- Hysteresis at Inputs to Improve Noise Margin
- PNP Inputs Reduce Loading
- 3-State Outputs Drive Bus Lines
- Inputs and Outputs Opposite Side of Package, Allowing Easier Interface to Microprocessors
- Input Clamp Diodes Limit High-Speed Termination Effects

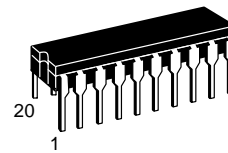
LOGIC AND CONNECTION DIAGRAMS DIP (TOP VIEW)



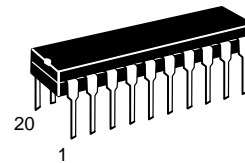
SN54/74LS540 SN54/74LS541

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

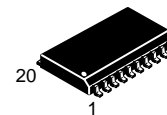
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

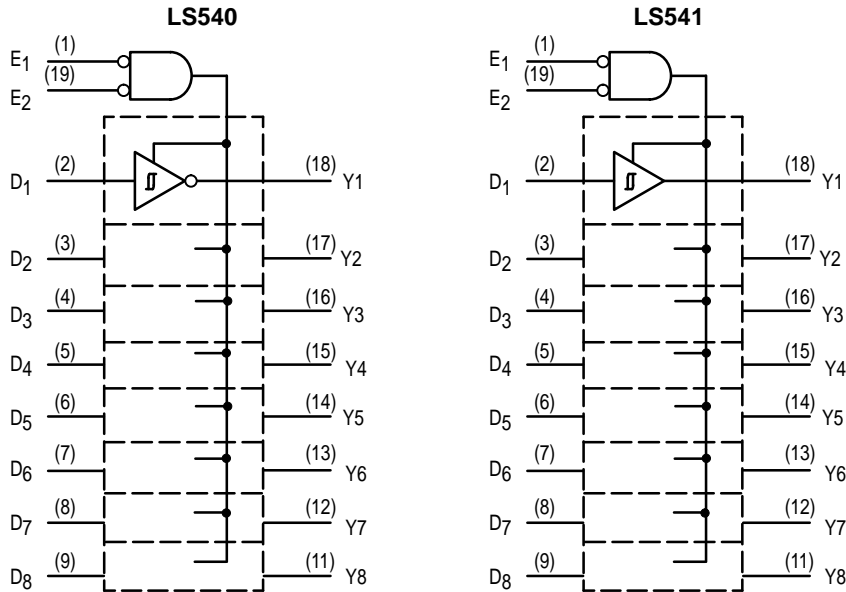
SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54 74			-12 -15	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

SN54/74LS540 • SN54/74LS541

BLOCK DIAGRAM



INPUTS			OUTPUTS	
E ₁	E ₂	D	LS540	LS541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.4	3.4	V	V _{CC} = MIN, I _{OH} = -3.0 mA
		54, 74	2.0		V	V _{CC} = MIN, I _{OH} = MAX, V _{IL} = 0.5 V
V _{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	I _{OL} = 12 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74	0.35	0.5	V	
V _{T+} -V _{T-}	Hysteresis	0.2	0.4		V	V _{CC} = MIN
I _{OZH}	Output Off Current HIGH			20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V
I _{OZL}	Output Off Current LOW			-20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.2	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)	-40		-225	mA	V _{CC} = MAX
I _{CC}	Power Supply Current Total, Output HIGH	LS540		25	mA	V _{CC} = MAX
		LS541		32	mA	
	Total, Output LOW	LS540		45	mA	
		LS541		52	mA	
	Total Output 3-State	LS540		52	mA	
		LS541		55	mA	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS540 • SN54/74LS541

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH}	Propagation Delay, Data to Output	LS540	9.0	15	ns	V _{CC} = 5.0 V C _L = 45 pF R _L = 667 Ω
t _{PLH}		LS541	12	15		
t _{PHL}		LS540	12	15		
t _{PHL}		LS541	12	18		
t _{PZH}	Output Enable Time to HIGH Level	LS540	15	25	ns	
t _{PZH}		LS541	15	32		
t _{PZL}	Output Enable Time to LOW Level	LS540	20	38	ns	
		LS541	20	38		
t _{PHZ}	Output Disable Time to HIGH Level	LS540	10	18	ns	C _L = 5.0 pF
		LS541	10	18		
t _{PLZ}	Output Disable Time to LOW Level	LS540	15	25	ns	
		LS541	15	29		

AC WAVEFORMS

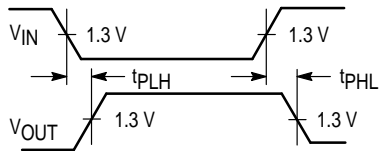


Figure 1

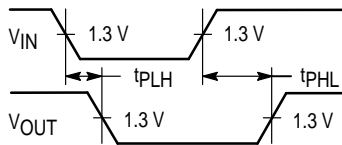


Figure 2

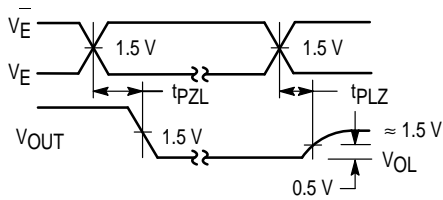


Figure 3

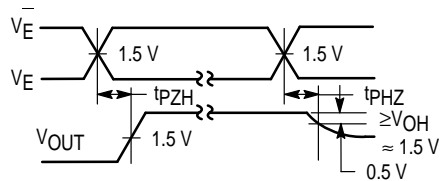
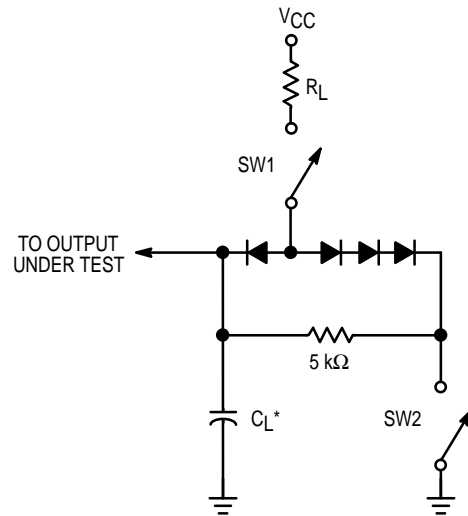


Figure 4



SWITCH POSITIONS

SYMBOL	SW1	SW2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PLZ}	Closed	Closed
t _{PHZ}	Closed	Closed

Figure 5